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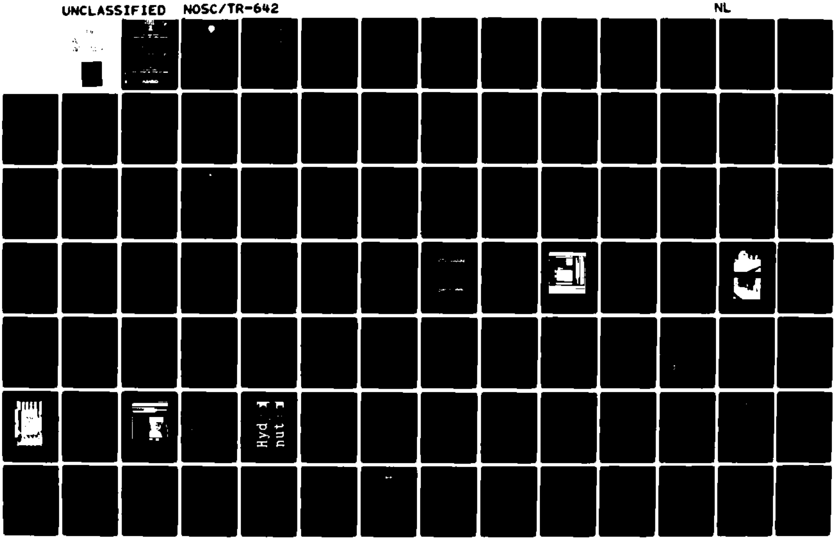

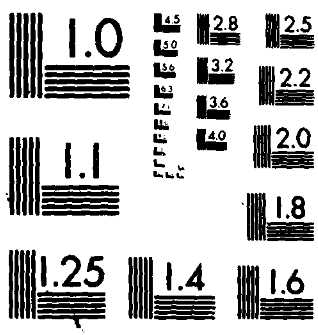

MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

NOSC TR 642

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NOSC TR 642

UNITED STATES POSTAL SERVICE

U.S. MAIL

AD A097493

SIXTH ANNUAL REPORT
ADVANCED MAIL SYSTEMS SCANNER TECHNOLOGY

#5 - A087436

Executive Summary and Appendixes A-E.

October 1980

Prepared by
NOSC Sensor Processing and Analysis Division (Code 732)
NAVAL OCEAN SYSTEMS CENTER
San Diego, California 92152

FOR
US POSTAL SERVICE
OFFICE OF ADVANCED MAIL SYSTEMS DEVELOPMENT

AMSD

NAVAL OCEAN SYSTEMS CENTER, SAN DIEGO, CA 92152

AN ACTIVITY OF THE NAVAL MATERIAL COMMAND

SL GUILLE, CAPT, USN
Commander

HL BLOOD
Technical Director

ADMINISTRATIVE INFORMATION

This report contains a summary of work sponsored by the Office of Advanced Mail Systems Development, Research and Development Department of the US Postal Service, Rockville, Maryland 20852, under US Postal Service Agreement 104230-77-T-1604. The authorized USPS Technical Representatives are J McGinn and A Kegel. The principal NOSC investigator is Frank C Martin of the Signal Analysis and Image Processing Branch, NOSC Code 7323. Associate investigators are Lee A Wise, Ronald J Wagar, and Robert W Basinger, also of Code 7323. Thomas R Little formerly of the same code participated on the program until May 1980. Dr John A Roese of Code 7123 and Waldo R Robinson of Code 8235 also made major contributions to the project. Charles E Winterbauer of Code 7323 provided consulting assistance in the area of image data compressibility. This report is a compilation of data presented by all team members and was approved for publication in October 1980.

Released by
RL Petty, Head
Sensor Processing and
Analysis Division

Under authority of
RE Shutters, Head
Surface/Aerospace
Surveillance Department

METRICATION

Refer to American Society for Testing and Materials Standard for Metric Practice, ASTM designation E380-76, IEEE Std 268-1976, for metric equivalents and conversion factors for units used in this report.

DISCLAIMERS

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REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER: NOSC Technical Report 642 (TR 642)

2. GOVT ACCESSION NO.: AD-A097 493

3. RECIPIENT'S CATALOG NUMBER: Annual rept.

4. TITLE (and Subtitle): ADVANCED MAIL SYSTEMS SCANNER TECHNOLOGY. ~~Sixth Annual Report~~ Executive Summary and Appendixes A-E.

5. ~~TYPE OF REPORT & PERIOD COVERED~~: ~~Annual~~, 5 October 1979 — 4 October 1980

6. PERFORMING ORG. REPORT NUMBER:

7. AUTHOR(s): NOSC Sensor Processing and Analysis Division (Code 732)

NOSC/TR-642

8. CONTRACT OR GRANT NUMBER(s): Agreement 104230-77-T-1604

9. PERFORMING ORGANIZATION ~~NAME AND ADDRESS~~: Naval Ocean Systems Center, San Diego, California 92152

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: O, USPS, O (NOSC EE25)

11. CONTROLLING OFFICE NAME AND ADDRESS: Office of Advanced Mail Systems Development, US Postal Service, 11711 Parklawn Ave, Rockville, MD 20852, Attn: Mr. A Kegel, Program Manager

12. ~~REPORT DATE~~: October 1980

13. NUMBER OF PAGES: 140

14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office):

15. SECURITY CLASS. (of this report): Unclassified

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE:

16. DISTRIBUTION STATEMENT (of this Report): Approved for public release; distribution unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report):

18. SUPPLEMENTARY NOTES: See reverse

19. KEY WORDS (Continue on reverse side if necessary and identify by block number):

Charge coupled devices	Image storage	Self-scanned arrays
Data compression	Optical scanning	Solid-state scanners
Image acquisition	Photodiodes	Video processing
Image processing	Run length coding	

20. ABSTRACT (Continue on reverse side if necessary and identify by block number):

The objective of the effort described herein is to provide technical consultation, equipment, and support services to the US Postal Service which will contribute to the development of the system definition of a new-concept processing system, the Electronic Message Service (EMS). Included in the scope of effort are investigations of high-speed image scanning technology, image frame memory storage, and image enhancement; and the fabrication of a scanner/frame-store memory test assembly. The sixth annual report briefly describes the individual efforts of the reporting period in an executive summary and provides in-depth data in five appendixes: Appendix A, Advanced Compressibility; Appendix B, Improved Technology Evaluation; Appendix C, Data Capture; Appendix D, Image Capture and Analysis System Upgrade and Operation; and Appendix E, TDI CCD Imager Status.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE
S/N 0102-LF-014-6601

UNCLASSIFIED
SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

18. Previous annual reports:

First Annual Report, Advanced Mail Systems Scanner Technology, Naval Electronics Laboratory Center (NELC) TR 1965, 22 October 1975, DTIC AD A020175

Second Annual Report, Advanced Mail Systems Scanner Technology, NELC TR 2020, October 1976, volume 1 (Executive Summary and Appendixes A-F), DTIC AD A039962; volume 2 (Appendix G: Proprietary Supplement, High Speed Imaging Device), DTIC AD B018468L (now released for unlimited distribution)

Third Annual Report, Advanced Mail Systems Scanner Technology, NOSC TR 170, October 1977, DTIC AD A051508

Fourth Annual Report, Advanced Mail Systems Scanner Technology, NOSC TR 358, October 1978, DTIC AD A070546

Fifth Annual Report, Advanced Mail Systems Scanner Technology, NOSC TR 520, October 1979, DTIC AD A089436

Also see:

CCD Page Reader for Mail-Scanning Applications, Final Report for period 15 March 1976 to 15 May 1977, RCA Princeton Laboratories Report PRRL-77-CR-42, DTIC A062399

Available from:
Defense Technical Information Center
Cameron Station
Alexandria, VA 22314

OBJECTIVES

1. Provide the US Postal Service the technical consultation, equipment, and support services which will contribute to the development of the system definition of a new-concept processing system, the Electronic Message Service System (EMSS). Include in this scope of effort (1) investigations in scanner technology, image frame memory storage, and image enhancement, and (2) the design and fabrication of a scanner/frame-store memory test assembly.

2. Contribute to the selection of the most optimum imaging devices and techniques for high-speed image acquisition. Provide reliable designs of high-speed image processing logic which will preserve the quality of the image while reducing the image storage and transmission requirements and minimizing vulnerability of the image information to noise during processing, transmission, and reproduction.

3. Act as technical consultants to the USPS Office of Advanced Mail Systems Development in preparing technical requirements and statements of work and evaluating technical proposals and contractor performance; and perform technical evaluation of contractor-produced developmental equipment.

RESULTS

1. The ICAS has been a highly productive system during FY80. Because of late completion of final hardware memory and peripheral interfaces, the data for all FY79 reports were accumulated in the first and second quarters of FY80.

2. A few new high-performance peripherals were added to ICAS during FY80, including the Tektronix 4054 Graphic Computing System, the 4641 Matrix Printer, the 4662 Interactive Digital Plotter, and a second 4907 File Manager. These provide versatile high-speed outputs for ICAS and an off-line software program development capability.

3. Major improvements to ICAS software routines were added during the year, including the integration of the above peripherals. An assembler program was written for preparing ICAS software. Numerous routines were written for the color display interface, compressibility studies, and image manipulation.

4. Reports of significance on compressibility, improved technology evaluation, advanced data capture, ICAS upgrade and operation, and TDI CCD imager status were generated. These are included in this report as appendixes.

5. Imagery support tasks completed during the year included 200-by-200-pel and 300-by-300-pel scans for JPL compression studies, orthogonal scans of images, and participation in proposal evaluations.

FUTURE NOSC PLANS

IMAGE ACQUISITION STUDIES

1. Complete the conversion for 8-bit data.
2. Interface and evaluate the RCA TDI CCD.

3. Incorporate and evaluate the Hardware Illumination Corrector and Hardware Edge Enhancer.

4. Generate specifications for and procure a Video Storage and Display System.

5. Evaluate document classification algorithm with a modest-size data base.

6. Perform color acquisition studies.

7. Investigate address and bar code reading.

MASS MEMORY TECHNOLOGY

1. Collect performance data on tape, disk (hard, floppy, and optical), bubble, and RAM memories.

2. Provide a memory technology assessment.

3. Generate a tradeoff matrix for buffer memories.

4. Study memory control technology for information storage and retrieval (ISAR), sorts, merges, linked lists, etc.

5. Generate a tradeoff matrix for memory control applications.

IMAGERY COMPRESSION TECHNOLOGY

1. Continue investigation of transmission algorithms.

2. Study mass storage compression algorithms.

3. Initiate error detection and correction (EDAC) study.

4. Establish a contract for compression studies.

5. Study character and shape recognition.

CONTENTS

CONTENTS

GLOSSARY

GLOSSARY

ac	Alternating current
A/D	Analog to digital
address	Peripheral device selection or memory location specification
ALU	Arithmetic/logic unit
AMSD	Office of Advanced Mail Systems Development
AMSST	Advanced Mail Systems Scanner Technology
ASCII	American Standard Code for Information Interchange
AWG	American wire gage
baud	Effective bit rate in bits per second
bit	The smallest piece of digital information – either 0 or 1
bit serial	The bits of a character are transmitted serially
bootstrap	A built-in function which eases system start-up
B/W	Black/white
byte	A logical group of bits (8 is standard)
CCD	Charge-coupled device
CCPD	Charge-coupled photodiode
CPE	Central processing element
CPU	Central processing unit
CRT	Cathode ray tube
CTF	Contrast transfer function
D/A	Digital to analog
DBSC	Data bus switch card
dc	Direct current
DCC	Display control card
DEC	Digital Equipment Corporation
DIA	Digital image analyzer
DIP	Dual in-line package
DMA	Direct memory access
DoD	Department of Defense
DOS	Disk operating system
DPCM	Differential pulse code modulation
EAROM	Electrically alterable read-only memory
ECL	Emitter-coupled logic
EDAC	Error detection and correction
EDM	Engineering development model
EM	Engineering model
EMSS	Electronic Message Service System
FCU	Format control unit
FDS	First-difference statistics
FET	Field effect transistor
FFT	Fast Fourier transform
FSM	Frame-store memory
Fetch	Microroutine which retrieves MCU instructions from program memory

file	On magnetic tape, a grouping of logical records
filemark	A logical gap between tape files
firmware	System control by use of ROMs and a microprogram sequencer
fpf bit	Front-panel fetch bit; indicates that MCU instruction is from front panel
FSM	Frame-store memory
FY	Fiscal year
GFE	Government furnished equipment
GOMAC	Government Microcircuits Applications Conference
GPIB	IEEE STD 488-1975 general-purpose interface bus for asynchronous data communications
Gray code	A binary code in which only one bit changes at each increment
HCU	Hard-copy unit
HEE	Hardware edge enchancer
HIC	Hardware illumination corrector
Hz	Hertz; cycles per second
IC	Integrated circuit
ICAS	Image Capture and Analysis System
IEEE	Institute of Electrical and Electronics Engineers
interrecord gap	Physical space between magnetic tape logical records
I/O	Input/output
ISAR	Information storage and retrieval
JPL	Jet Propulsion Laboratory
k	1024
kW	Kilowatts
LDTB	Large drum test bed
LED	Light-emitting diode
LFPM	Linear feet per minute
LIES	Laboratory Image Exploitation System
listener	A device which may receive data on the GPIB
logical record	A logical grouping of data on magnetic tape. In an image, a video line is treated as a logical record
LSI	Large-scale integration
M	Mega-; million
machine language	Operation instructions interpretable by the machine being operated
macroinstruction	A machine language instruction which initiates a sequence of basic machine operations
macrolevel	A level at which an operator may directly communicate with a machine; ie, machine language level
macroprogram	A logical sequence of macroinstructions
MARB	Memory address register bus
MC	Master controller
MCU	Memory control unit
MDB	Multiplexed data bus
message	On the GPIB, a sequence of data and/or control operations transmitted

MIC	Memory interface card
MICC	Memory interface control card
microaddress	Micromemory address
microcode	Bit-by-bit implementation of microinstructions
microcontrol	Control of individual hardware resources by use of a microprogram structure
microinstruction	A basic machine operation instruction containing control for all hardware resources (eg, data paths, registers, ALUs)
microlevel	Hardware direct-control level
micromemory	Memory (usually ROM) which contains microinstructions
micromemory address	Specification of location within a micromemory
microprogram	A logical sequence of microinstructions
microroutine	A microprogram or part thereof
MIU	Memory interface unit
MOS	Metal oxide semiconductor
MSB	Most significant bit
MTBF	Mean time between failures
MTF	Modulation transfer function
n	Multiplex ratio
NASA	National Aeronautics and Space Administration
NELC	Naval Electronics Laboratory Center
nm	Nanometre
NOSC	Naval Ocean Systems Center
ns	Nanosecond
NTC	National Telecommunications Conference
OCR	Optical character recognition
page	An 8 1/2-by-11-inch acquired image or original copy
PBS	Pel brightness statistics
PC	Personality chassis; printed circuit
PCR	Print contrast ratio = $(r_{max} - r_{min})/r_{max}$
pel	Picture element
pixel	Picture element
PPHE	Printer and paper-handling equipment
PPHE/IU	Printer and paper-handling equipment/input unit
PPE	Printer/plotter equipment
PPP (P^3)	Plain paper printer
program	Sequence of machine instructions
PROM	Programmable read-only memory
PW	Public Works (Department)
r	Reflectivity
RAC	Relative address coding
RALU	Register arithmetic logic unit
RAM	Random-access (read/write) memory
RCA	Radio Corporation of America
record	Logical record

RFP	Request for proposal
RLC	Run length coding
RLS	Run length statistics
ROM	Read-only memory
s	Second
SAR	Synthetic aperture radar
SDC	System Development Corporation
SDTB	Small drum test bed
SFI	Spatial frequency identification
SID	Silicon imaging device
SLS	Side-look sonar
SOW	Statement of work
SPADE	Storage, processing, and display equipment
SPIE	Society of Photo-Optical Instrumentation Engineers
t_{mac}	Memory access time
t_{mcy}	Memory cycle time
talker	A device which may transmit asynchronous data on the GPIB
TDI	Time-delay and integration
TDMA	Time-division multiple access
three-wire handshake	The Hewlett-Packard patented method of guaranteeing asynchronous communication capability on the GPIB
TSB	Tristate buffer
TTL	Transistor-transistor logic
UDK	User definable key
USASCII	American Standard Code for Information Interchange
USPS	United States Postal Service
UV	Ultraviolet
VMOS	Vertical metal oxide semiconductor
VTS	Video transmission system (Navy)
word	A grouping of 1 or more bytes (in the MCU, a word contains 6 bytes, or 48 bits)

RELEVANCE TO DoD MISSION

RELEVANCE TO DoD MISSION

Approval for the US Postal Service (USPS) Electronic Message Service System (EMSS) has been signed by the President for the high-speed distribution of letter mail. The concept of EMSS includes the very high-speed transmission of digital information throughout the United States on a vast network of available transmission systems. When instrumented, it will become the second largest communication and information exchange system in the US. The requirements for speed, privacy, security, reliability, and area of coverage closely parallel the requirements for several military information dissemination networks. Participation on interface aspects of the system such as imagery and facsmile transmission, buffer storage, and compressibility provides the Navy intimate familiarity. Because of this familiarity, the Navy may assist in utilization of the network for military purposes in a time of national need.

Both DoD and USPS have a requirement for high-speed dissemination of imagery-like data, and there is a multifold increase in DoD use of high-speed digital imagery transmission and soft-copy display. The expected size of digital images is increasing to include areas up to 4000 by 4000 picture elements (pels) and larger. Military requirements for continuous-tone images (photographs) and color images are placing ever-increasing demands on acquisition, storage, and display technology to provide the user with the efficient analytic tools necessary to make rapid and accurate decisions and conclusions. Hard-copy documentary records of a desirable subset of the displayed data are often required. The EMSS encompasses the same technical requirements: the need for digitization of hard-copy imagery as inputs, the buffer storage of imagery data, the transmission of compressed or uncompressed imagery data, the soft-copy display of images, and the decompression and final hard-copy printing of the received image.

The USPS Image Capture and Analysis System (ICAS) has been designed to acquire and interchange data with the NOSC video testbed in the Display Equipment Development Branch, Code 8247. Digital image tapes can be generated by scanning or converting tapes from other sources to a format compatible with the Laser Recording System located in the Marine Corps and Special Systems Branch, Code 8125. An image has been scanned, digitized, and analyzed for Code 823. Radar tapes in various configurations from Codes 8215 and Code 8247 have been accepted by ICAS and displayed. Other digital nonliteral imagery such as lofargrams, side-look sonar (SLS), and synthetic aperture radar (SAR) can be digitized, stored, analyzed, and displayed by ICAS.

A large high-speed charge-coupled device (CCD) which can operate in the time-delay and integration (TDI) mode is being developed for the program. This single device is capable of acquiring full-page data at a rate of 20 pages per second. The high performance of the device makes it applicable for telereconnaissance, teleguidance, battlefield surveillance, and intrusion detection as well as document imaging. Successful operation of the first-phase device was witnessed at the contractor's facility and a second contract is underway for refinement and advancement of this important work.

The very high-speed requirement resulting from the data rate standards established by the USPS have resulted in the need for high-performance special microprocessor architecture for the acquisition, correction, enhancement, storage, and display of the imagery. Very little of the work within the DoD and academic communities involves high-speed, real-time hardware and algorithm developments which support current military applications such as those listed below:

- ocean surveillance
- telereconnaissance

- teleguidance
- battlefield surveillance
- intrusion detection
- image transmission system
- image interpretation
- pattern/character recognition
- word processing

EXECUTIVE SUMMARY

INTRODUCTION

The major goal of the total Scanner Technology Program is to identify and resolve the problems associated with producing digital equivalent images from a wide variety of hard-copy documents at very high speed. Major goals for the project at NOSC can be divided into the following three categories:

1. High-quality image acquisition

- Either orientation of 8 1/2-by-11 inch documents
- Up to 91.8 megapels per second
- Typed, handwritten, or continuous-tone images
- Resolution up to 200 by 200 or 300 by 300 pels per inch
- Data rates up to 735 megabits per second
- Monochrome or color images

2. Image enhancement

- Edge enhancement
- Nonlinear video techniques
- Thresholding
- Color filtering

3. Picture bandwidth compressibility techniques

- Run length encoding
- Walsh, slant, Fourier encoding
- Block void encoding

This report is the sixth in a series of annual summary reports and covers work during the period October 1979 through September 1980. Titles and sources of previous reports are given in section 18 of the Report Document Page (DD 1473) in the front of this report. Again this year, the work was reasonably well balanced among the four categories of hardware, software, support, and documentation. Incorporation of peripherals and upgrades in ICAS caused slippage of completion of several FY79 deliverables until the first and second quarters of FY80. Consequently, the documentation effort for this reporting period was much heavier than normal. Since its last major upgrade about a year ago, ICAS has been a highly productive and reliable system and with the generation of this report all due deliverables are complete.

1980 TASKS

The accomplishments for the year ending 3 October 1980 are presented in this section in summary form in four general task subdivisions.

HARDWARE ACCOMPLISHMENTS

EIGHT-BIT D/A CONVERTER

The digital-to-analog (D/A) converter used for several years to convert the stored 6-bit digital imagery to analog video has been an experimental two-of-a-kind (model 8123), 10-bit, 100-MHz hybrid converter made for the NOSC Display Division by the Motorola Government Electronics Division. To avoid dependence on nonreplaceable subassemblies, this D/A was replaced with an Analogic model MP 8308 ECL high-speed composite video D/A. This converter converts 8-bit data at rates up to 100 megabytes per second.

EIGHT-BIT A/D CONVERTER

ICAS analog-to-digital (A/D) conversion in the past has been performed with four Phoenix Data 6-bit A/D converters, three of which are operable to 60-M and one of which is operable at 100-M conversions per second. Planned experiments require conversion of imagery data at 8-bit accuracy. For this reason, a conversion chassis was fabricated using the TRW TDC-1007J A/D converter. This unit converts analog video to 8-bit digital form at rates up to 20-M (guaranteed) or 30-M (typical) conversions per second.

LAMP HOUSE PROCUREMENT

Results of the Fairchild Scanhead evaluation showed that the Fairchild illumination source for document scanning was superior to the original NOSC/ICAS source. Therefore, a procurement for a similar unit was initiated. The new unit will have cylindrical lenticular lenses and forced-air cooled lamp housings. The unit operates on 20-kHz ac power rather than dc. This will minimize changes of lamp characteristics due to mercury migration and uneven phosphor changes. Delivery is expected in January 1981.

FILM ILLUMINATION FLATTENER

The slit-aperture fluorescent lamps in the large drum test bed do not provide a uniform level of illumination across the document page. A full width, variable density film negative of the illumination profile was generated and attached to the lamps. Although there was some reduction in the overall reflected energy, the profile was flattened to a considerable extent. This technique may be applied to the future Fairchild illumination assembly.

EIGHT-BIT PERSONALITY MODULE

Investigations into the acquisition of 8-bit pel data require that the ICAS data memory word format be modified from eight each 6-bit words to six each 8-bit words. This is being accomplished by designing a new module for the personality chassis which can be used for either 6-bit or 8-bit data by selection with a dual in-line package (DIP) switch. The design is complete and fabrication of the module is in progress.

CCD143 DEVICE AND DRIVER

Fairchild has produced an improved 2048-element, high-speed linear image sensor, the CCD143. The photoelement size is the same as the older line imagers, 13μm (0.51 mil) centers.

The unit provides two separate output ports, each of which operates at up to 10 megapixels per second. This single device can support acquisition of 10.24 inch-wide documents scanned at 200 by 200 pels per inch at a five-page-per-second rate. The new units have higher sensitivity, an enhanced blue response, and a lower dark signal. Two CCD143 devices were procured, and a driver board is being designed to operate the device at its maximum operating speed.

HIC and HEE CONTRACT

In February an unsolicited proposal was received from Data/Ware Development Inc to design and fabricate a Hardware Illumination Corrector (HIC) and Hardware Edge Enhancer (HEE) equipment. The HIC is placed in series with the data path from the A/D converter to the personality chassis in the ICAS image acquisition port. The HIC provides storage for a 4096-pel, 10-bit digital "white standard" profile which is loadable from ICAS. Once the profile is loaded, the HIC is capable of providing illumination-corrected pel data to ICAS at a rate up to 20.5 megapels per second.

The HEE operates in series immediately following the HIC and with a high-speed pipeline circuit applies the three-by-three edge enhancement algorithm to image data at a 20.5-megapel-per-second rate. Since 20.5 megapels per second is only a five-page-per-second acquisition rate, design considerations have been given to allow for future multichannel operations with additional units.

NEW LDTB SCANNER TABLE

At the request of the sponsor, a high-performance large drum test bed (LDTB) scanner table was fabricated as GFE to RCA Princeton for evaluation of the time-delay and integration (TDI) charge-coupled device (CCD) development contract. Numerous upgrades in the mechanical design were added to the older design drawings before the scanner table was fabricated. The drum was widened to accommodate 11-inch documents and the centerline of the bearings was raised to 7 inches instead of 2 1/2 so that the TDI CCD and support electronics can be mated without special interfaces.

This new LDTB offered so many advantages it was decided to upgrade the NOSC version to the same performance level. With the new version, the original "dog-house" which was formerly located above the scanner has been replaced by a durable rack-mount rolling table upon which the scanner table is located. The lamp power supply and all future imaging device drivers plus the A/D converters can now be placed in accessible close proximity to the imager.

SOFTWARE ACCOMPLISHMENTS

ICAS SOFTWARE UPGRADES

Much of the software effort during the reporting period has been expended to improve the utility, processing speed, and accuracy of ICAS image processing.

COMTAL INTERFACE

Simple software was written in November 1979 to allow a transfer of image information from the ICAS frame-store memory (FSM) via the memory control unit (MCU) to the Comtal image refresh memory. In June 1980 this software was upgraded significantly to allow an exchange of image data between ICAS and the Comtal in either direction. The software allows an operator to select any 512-by-512 area of the 1728-by-2200 ICAS image memory and to transmit the data to any of the three color memories of the Comtal. Function table information can also be transmitted between the equipment.

DICOMED COLOR IMAGE RECORDER INTERFACE

In January software was added to ICAS to control the Dicomed recorder for printing color images. The software allows the transmission of data from the ICAS frame-store memory via the MCU to the Dicomed. Software test images were also generated to balance the color sensitivity adjustments by using grey-scale intensity wedges.

ARRAY PROCESSING UPGRADES

Array processing software for ICAS was initially described in Appendix A of the October 1979 annual report. The major functions include two-vector arithmetic operations, vector-scaler arithmetic operations, and statistical analysis of vectors. Specific examples of two-vector operations are point-by-point addition and point-by-point multiplication of each vector element by a constant. Statistics include such values as arithmetic mean, mean deviation, and mean-square difference. The software routines for these functions were re-examined and several improvements were made, including faster multiply and divide routines, and easier manipulations of vector addresses.

MINIFICATION

A full-page 8 1/2-by-11 inch image acquired at 200 by 200 pels per inch contains 3.7 million pels. Display of this image at full resolution at a 30-Hz rate requires a video bandwidth in excess of 112 megapels per second (with retrace overhead, closer to 140 megapels per second). For this reason, a minify algorithm was written to sum and normalize "m"-by-"n" arrays of pels into a smaller representation of the image. This image now contains $(3.74 \times 10^6)/(m \times n)$ pels and can be displayed on a standard TV monitor having conventional line rates and bandwidth. This software was improved to accelerate the process in ICAS and to provide more freedom in the choice of starting coordinates and values of m and n.

DISPLAY SOFTWARE UPGRADE

The display software upgrade included the addition of a cursor display feature. A cursor whose shape can be arbitrarily defined within a 16-by-16 array can be superimposed on the image presented on the CRT monitor. This presentation is "nondestructive" in that the image data are again viewable when the cursor is moved away.

ASSEMBLER SOFTWARE

Instructions recognizable by ICAS are contained in 48-bit computer words. Writing programs in this form is laborious. For this reason an assembler program has been written and is being upgraded frequently. The assembler is written in BASIC language and will run on the Tektronix 4051 graphic computing system and its associated Tektronix 4907 file manager. The software allows programs to be written in terms of mnemonics such as ADD, SHIFT, and JUMP. It also allows comment fields to be added and labels to be added to code lines. Thus, with English language inputs, 48-bit computer word instruction lists can be generated for use on the ICAS.

FFT PLOTTING SOFTWARE

One of the support service requests from the sponsor was a series of scans of blank bond paper and a typed letter. The results of the scans were to be analyzed by use of fast Fourier transforms (FFTs). The FFTs were run on a NOSC DEC PDP 11/70. In order to plot the results, software was written to provide the formats, legends, and coordinate data.

IMAGE ROTATION

Software was written to allow images to be rotated through quadrant angles in the frame-store memory. The program permits images or portions of images to be reoriented for display purposes. A more general algorithm for rotation about a point at any given angle was given a cursory examination but was not considered necessary for immediate Postal Service applications.

MUIRHEAD 75C COMPRESSION ALGORITHM

Other related work at NOSC revealed that the British have developed a compression algorithm known as Muirhead 75C with good resistance to channel noise. Although the details are considered proprietary, NOSC was given permission to develop the software to compress and decompress image data using the algorithm rules. Results of images compressed via this technique as compared to run length algorithms are discussed in appendix A. The results are favorable for the Muirhead 75C approach with its full overhead provisions as opposed to conventional run length algorithms with no overhead.

A/D CONVERTER TEST UPGRADES

Minor modifications to the A/D converter characterization software were required when testing the TRW 8-bit converters. These converters operate between -2.0 and 0.0 volts. The Phoenix Data converters operated between −2.0 and +2.0 volts. The software, when upgraded, was written to accommodate a selectable voltage input range.

SUPPORT ACCOMPLISHMENTS

COMPRESSION TAPES GENERATION

The USPS entered into an agreement with NASA/JPL for an image compression study. NOSC was requested to support the study by providing image tapes. The tapes included images scanned at 200 by 200 and 300 by 300 pels per inch. Four illumination-corrected images, each 8 1/2 by 11 inches, scanned at 6-bits per pel and thresholded for each of the two resolutions, were provided.

RCA TDI CCD IMAGER SUPPORT

NOSC has provided considerable support to USPS on a contract for the development of a high-speed time-delay and integration (TDI) charge-coupled device (CCD) imager. Technical support has been provided at the kick-off meeting and several progress visits at RCA. NOSC also hosted an interface workshop at which the intricate details of signal and control paths between the imager electronics and ICAS were resolved. A complete large drum test bed (LDTB) fabricated by the NOSC/PW machine shop and assembled and wired by the project technician was shipped to RCA for evaluation of imager performance.

PLAIN PAPER PRINTER PROPOSAL EVALUATION

Members of the NOSC team evaluated proposals and attended oral discussions resulting from a USPS plain paper printer (P^3) RFP. Several discussions with the successful bidder have been held since the award.

MASTER CONTROLLER PROPOSAL EVALUATION

Specifications were generated by USPS for a study of the master controller (MC) architecture needed for the Rockville Laboratory during the experimentation of EMSS. Members of the NOSC team evaluated proposals and attended a USPS evaluation meeting resulting from the USPS MC RFP. Proposals were ranked in accordance with scoring factors, and resulting ratings were discussed at the USPS laboratories.

FAIRCHILD SCANNER PROPOSAL EVALUATION

A Fairchild proposal for the engineering model (EM) scanner was evaluated and comments were provided to USPS.

DOCUMENTATION

As mentioned, because of delays in readying ICAS for operation with the advanced memory interface unit (MIU), three of the four appendixes for the 1979 annual report were actually generated during the FY80 project activities. The first three documents listed below, written in FY80, were included as appendixes in the FY79 Report.

COLOR IMAGING REPORT

As appendix B in the FY79 report, the summary described work accomplished in acquiring, correcting, analyzing, and printing color images.

DATA DISPLAY SYSTEMS PERFORMANCE ANALYSIS

For the Naval Weather Prediction Service, the progress of CRT exposure with wet process transparency development was compared with the newer Harris laser exposure and dry development process for uniformity and resolution. The newer acquisition system was found to be superior to the older one. This work is reported as appendix C of the FY79 report.

FAIRCHILD EDM EVALUATION REPORT

The Fairchild Weston engineering development model (EDM) scanner was evaluated for performance parameters beyond the specified and design goal operating parameters. The results of this study showed that good quality, continuous-tone images can be acquired with the EDM scanner at speeds up to 8.5 pages per second. Details are included as appendix D of the FY79 report.

ADVANCED COMPRESSIBILITY REPORT

This was the first SOW deliverable scheduled for the FY80 project. The British Muirhead 75C compression algorithm was reduced to ICAS software and used to compress and expand several images. The compression ratios using the 75C code with full overhead were compared to those using several run length algorithms without overhead. The Muirhead 75C algorithm compared favorably in compressibility with all other algorithms tested. No further compressibility experiments with ICAS are planned until the 8-bit A/D converter and hardware illumination corrector (HIC) are properly integrated into ICAS. The work is described in appendix A of this report.

IMPROVED TECHNOLOGY EVALUATION REPORT

This report, contained in appendix B, describes problems with the existing 6-bit A/D converter and Fairchild CCD121H imager. It also describes the progress and future integration plans for the 8-bit TRW A/D converter and Fairchild CCD143 imager.

DATA CAPTURE ADVANCED REPORT

Appendix C presents an approach for the generation of a document recognition algorithm. The principal purpose of the experiment was to generate a procedure which would identify a typed paged with a high degree of confidence, and to further classify documents into three categories. The categories are the plain typed page, other bilevel images capable of being thresholded and transmitted at 1 bit per pel, and continuous-tone images. The algorithm appears adequate to identify typed pages with fairly good confidence. In FY81, the process performance with a few dozen samples will be evaluated for consistency.

ICAS UPGRADE AND OPERATION REPORT

Appendix D provides a good description of the evolution of ICAS since the last reported detailed description in October 1977. Beneficial changes in memory storage and retrieval techniques for image acquisition, display, and dissemination to peripherals are discussed. Detailed plans for Scanner III are presented. Included are the plans for completely new clock driver and signal conditioning circuits for the new Fairchild 2048-element CCD143 linear imager. The accommodation for the 8-bit TRW A/D converter (whose preliminary performance characteristics are presented) is discussed. The new personality module for 6-bit or 8-bit data acquisition is also described.

TDI CCD IMAGER STATUS REPORT

Appendix E was written to document the present plans for integrating the RCA TDI CCD into our new Scanner III test bench. Meetings between NOSC and RCA have aided in defining the interface signals and timing requirements. Plans for the characterization and evaluation of the TDI imager are also given.

APPENDIX A:

ADVANCED COMPRESSIBILITY

by

Robert W Basinger

Code 7323

May 1980

CONTENTS

TABLES

INTRODUCTION

This report is a follow-up to the data compression reports contained in the second and third annual reports on Advanced Mail Systems Scanner Technology. At the time of those reports, there was no requirement for NOSC's development of USPS compression algorithms. Because of the availability and versatility of resources, however, it has become increasingly desirable for NOSC to pursue this line of investigation. There are several reasons supporting NOSC's continued investigation into data compression. First, as mentioned, resources at NOSC are both available and versatile. The NOSC data base is continually enlarged and image data can be obtained from numerous outside sources. In addition, data can be both accepted and generated in several different formats.

A second reason for studying compression is the possibility of reducing the storage requirement for digitized images. In line with this is a consequent reduction in the required transmission bandwidth. At the specified rate of 20 pages per second, the bandwidth required is approximately 504 MHz. Any reduction in this bandwidth would be beneficial.

The third reason for this study is to assess the validity of claims for high-compression-ratio algorithms made by private sector companies.

BACKGROUND

PREVIOUS NOSC WORK

The second annual report for the Advanced Mail Systems Scanner Technology (AMSST) investigation (ref 1) contained this project's first attempts at calculating compressibility for various algorithms. That report based calculations of compressibility upon straight run length statistics acquired through the digital image analyzer (DIA). Compression ratios were calculated for these data using 2-bit and 3-bit variable-length code and 4-bit and 6:3-bit fixed-length code algorithms.

A shortcoming of the first compression report resulted from the DIA's limitation to runs of 64 or less as well as the requirement for 12 separate passes through the image to accumulate all the run length statistics. For the third annual report for AMSST, these problems were overcome by the generation of a software analysis package which accumulated run length statistics in only three passes and for run lengths up to 13 824 (1728 x 8). With the increased capability, the compression ratio calculations were repeated, by using a variety of "meander" run length generation algorithms. By using the 2-bit and 3-bit variable-length encoding schemes, a large potential increase in compressibility was shown possible with the longer runs generated by the meander algorithms.

NEW INPUTS

Despite the improvements shown in the third annual report (ref 2), the calculations lacked any allowance for overhead; eg, line sync code or other error recovery information

1. Advanced Mail systems Scanner Technology Second Annual Report, NELC TR 2020, Oct 1976
2. Advanced Mail Systems Scanner Technology Third Annual Report, NOSC TR 170, Oct 1977

added to the image data. The current report contains this project's first efforts at the actual encoding of an image, including overhead, as opposed to calculations based upon run length statistics alone.

The current algorithm under investigation is known as code 75C. At the present time, the actual algorithm is proprietary to the British Ministry of Defence and may only be disclosed to Government agencies with prior approval. It may be stated, however, that the algorithm is based upon run lengths and contains error recovery capability. Permission has been given to disclose results (to be discussed later in the report) of a software simulation of the algorithm.

TESTS TO BE MADE

The primary objective of this report is to compare the results of the previously used compressibility calculation algorithms with the results of the actual compression of images.

Digitized copies of eight CCITT standard images were obtained. These images (1-8) were scanned at approximately 200 pels per inch and 1 bit per pel. It was decided to use these images as a basis for algorithm comparison because of their status as standards. It is hoped that this will allow future comparisons of algorithms tested by NOSC with algorithms tested by others. In addition, because the images are already digitized and thresholded, a major step in the procedure is eliminated.

The first step, then, was to perform a run length analysis on each of the eight images. Run lengths of 1 to 1728 were tabulated and stored on tape for use by each of the ratio calculation algorithms. The second step was to calculate and tabulate all ratios for each of the image-algorithm combinations. The final step was to perform the actual encoding using the 75C algorithm and tabulate the results.

SOFTWARE IMPACT

The software required to complete this report included the following:

1. Operator interaction. This software was required to allow the operator to select the operation or algorithm option to test. It also formatted the results into a readily human-usable form.

2. Compressibility calculation algorithms. The two fixed-length codes had been dropped from the software library following the first test, which showed poor results. These two calculation algorithms were revived and made a permanent part of the software library.

3. 75C encoding and decoding. In accordance with the encoding/decoding rules provided by the British Ministry of Defence, the algorithm was simulated. The two-way encoding/decoding test affords the opportunity both to verify that the algorithm was correctly implemented and to assess the ability of the algorithm to provide an error recovery capability.

THE ALGORITHMS. The compression ratio algorithms used were 2-bit and 3-bit variable-length codes and 4-bit and 6:3-bit fixed-length codes. The only differences between the two variable-length codes are a slight reallocation of code word lengths and an increased minimum code length as shown in table A1. The 2-bit code shows better compression for

IMAGE 1

THE SLEREXE COMPANY LIMITED

SAPORS LANE - BOOLE - DORSET - BH 25 8 ER

TELEPHONE BOOLE (945 13) 51617 - TELEX 123456

Our Ref. 350/PJC/EAC 18th January, 1972.

Dr. P.N. Cundall,
Mining Surveys Ltd.,
Holroyd Road,
Reading,
Berks.

Dear Pete,

Permit me to introduce you to the facility of facsimile transmission.

In facsimile a photocell is caused to perform a raster scan over the subject copy. The variations of print density on the document cause the photocell to generate an analogous electrical video signal. This signal is used to modulate a carrier, which is transmitted to a remote destination over a radio or cable communications link.

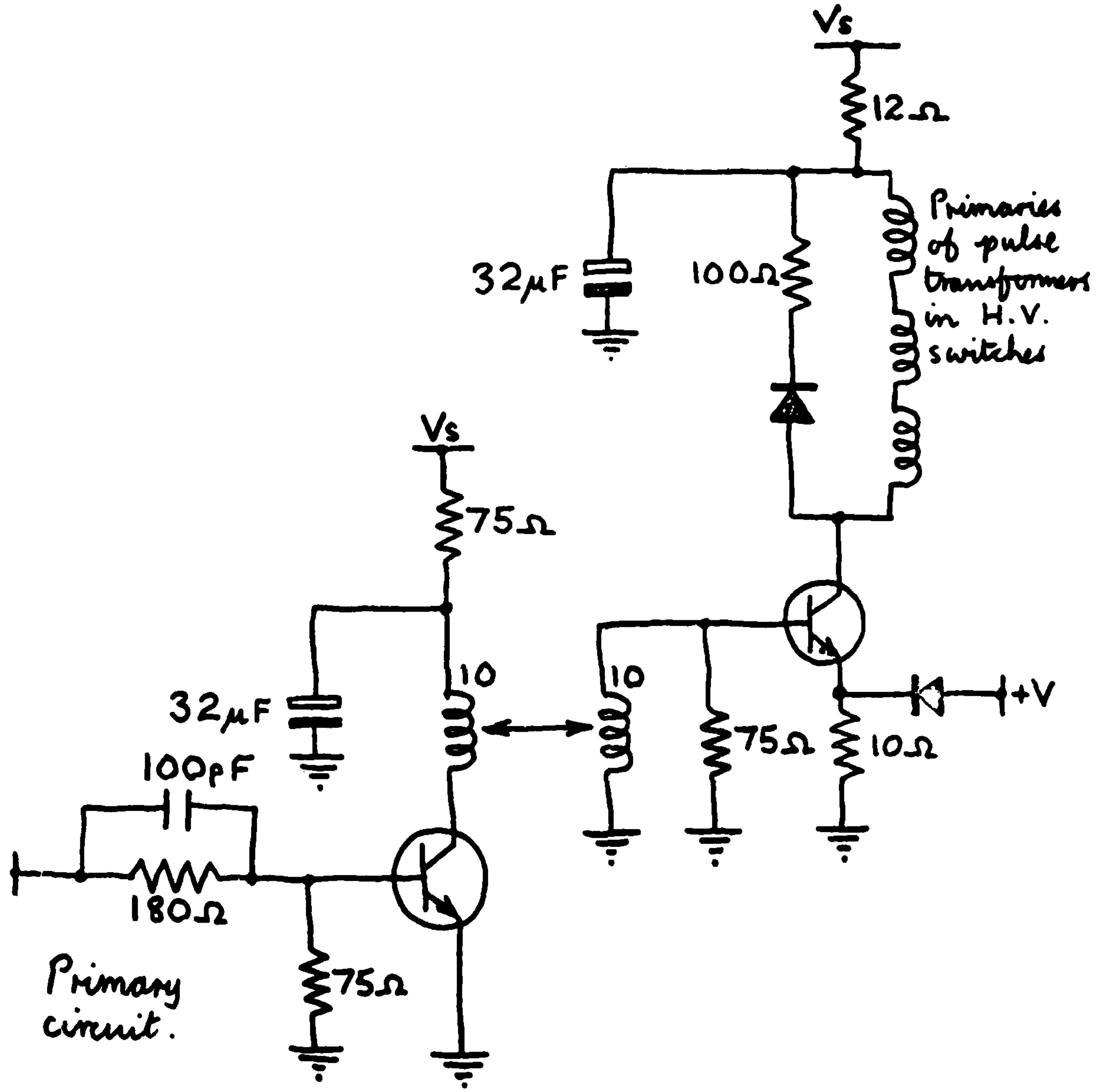
At the remote terminal, demodulation reconstructs the video signal, which is used to modulate the density of print produced by a printing device. This device is scanning in a raster scan synchronised with that at the transmitting terminal. As a result, a facsimile copy of the subject document is produced.

Probably you have uses for this facility in your organisation.

Yours sincerely,

Phil.

P.J. CROSS
Group Leader - Facsimile Research



This is current driver circuit.

Phil.

ÉTABLISSEMENTS ABCDEFG
SOCIÉTÉ ANONYME AU CAPITAL DE 300 000 F
30, RUE DU XVUTRSTBSL F 00000 NTBCLAG
Tél. : (35) 34.46.32 Adr. Tg. : NRVLJROLM
Télex : 31396 F IN : 716460070257
Transporteur (ou Transitaire)
M. M. DUPONT Frères
8 quai des biodfsh F 6000 NTBCLAG

Mot directeur

CLASSEMENT	FACTURE INVOICE	Exemplaire 15	
CODE CLIENT Z 04599	DATE 7-7-74	NUMÉRO 06	FEUILLET 01

Votre commande du 74-2-2 numéro 438
Notre offre AZ/B7 du 74-1-1 numéro 12

LIVRAISON
5, rue XYZ
99000 VILLE

FACTURATION
12, rue ABCD BP 15
99000 VILLE

DOMICILIATION BANCAIRE DU VENDEUR

CODE BANQUE　CODE GUICHET　COMPTE CLIENT

ORIGINE	TRANSPORTS DESTINATION	MODE
Pays 1	Etat 2	Air

PAYS D'ORIGINE　PAYS DE DESTINATION

CONDITIONS DE LIVRAISON　DATE 74-03-03

LICENCE D'EXPORTATION　NATURE DU CONTRAT (monnaie)

CONDITIONS DE PAIEMENT (échéance, %...) FAB

MARQUES ET NUMÉROS MARKS AND NUMBERS	NOMBRE ET NATURE DES COLIS : DÉNOMINATION DE LA MARCHANDISE NUMBER AND KING OF PACKAGES: DESCRIPTION OF GOODS	NOMENCLATURE STATISTICAL No.	MASSE NETTE NET WEIGHT MASSE BRUTE GROSS WEIGHT	VALEUR VALUE DIMENSIONS MEASUREMENTS
74.21.456.44.2 A	1 Composants	U 123/4	5 kg 8 kg	1400 X 13x10x6

QUANTITÉ COMMANDÉE ET UNITÉ QUANTITY ORDERED AND UNIT	N° ET RÉF. DE L'ARTICLE	DÉSIGNATION	QUANTITÉ LIVRÉE ET UNITÉ QUANTITY DELIVERED AND UNIT	PRIX UNITAIRE UNIT PRICE	MONTANT TOTAL TOTAL AMOUNT
2	AF-809	Circuit intégré	2	104,33 F	208,66 F
10	S8-T4	Connecteur	10	83,10 F	831,00 F
25	ZI07	Composant indéterminé	20	15,00 F	300,00 F

		Inclus	Non inclus
Costs	Débours		
Packing	Emballages		92,14
Freight	Transport		
Insurance	Assurances		
Total invoice amount	Montant total de la facture		1431,80

L'ordre de lancement et de réalisation des applications fait l'objet de décisions au plus haut niveau de la Direction Générale des Télécommunications. Il n'est certes pas question de construire ce système intégré "en bloc" mais bien au contraire de procéder par étapes, par paliers successifs. Certaines applications, dont la rentabilité ne pourra être assurée, ne seront pas entreprises. Actuellement, sur trente applications qui ont pu être globalement définies, six en sont au stade de l'exploitation, six autres se sont vu donner la priorité pour leur réalisation.
Chaque application est confiée à un "chef de projet", responsable successivement de sa conception, de son analyse-programmation et de sa mise en oeuvre dans une région-pilote. La généralisation ultérieure de l'application réalisée dans cette région-pilote dépend des résultats obtenus et fait l'objet d'une décision de la Direction Générale. Néanmoins, le chef de projet doit dès le départ considérer que son activité a une vocation nationale donc refuser tout particularisme régional. Il est aidé d'une équipe d'analystes-programmeurs et entouré d'un "groupe de conception" chargé de rédiger le document de "définition des objectifs globaux" puis le "cahier des charges" de l'application, qui sont adressés pour avis à tous les services utilisateurs potentiels et aux chefs de projet des autres applications. Le groupe de conception comprend 6 à 10 personnes représentant les services les plus divers concernés par le projet,et comporte obligatoirement un bon analyste attaché à l'application.

II - L'IMPLANTATION GEOGRAPHIQUE D'UN RESEAU INFORMATIQUE PERFORMANT

L'organisation de l'entreprise française des télécommunications repose sur l'existence de 20 régions. Des calculateurs ont été implantés dans le passé au moins dans toutes les plus importantes. On trouve ainsi des machines Bull Gamma 30 à Lyon et Marseille, des GE 425 à Lille, Bordeaux, Toulouse et Montpellier, un GE 437 à Massy, enfin quelques machines Bull 300 TI à programmes câblés étaient récemment ou sont encore en service dans les régions de Nancy, Nantes, Limoges, Poitiers et Rouen ; ce parc est essentiellement utilisé pour la comptabilité téléphonique.
A l'avenir, si la plupart des fichiers nécessaires aux applications décrites plus haut peuvent être gérés en temps différé, un certain nombre d'entre eux devront nécessairement être accessibles, voire mis à jour en temps réel : parmi ces derniers le fichier commercial des abonnés, le fichier des renseignements, le fichier des circuits, le fichier technique des abonnés contiendront des quantités considérables d'informations.
Le volume total de caractères à gérer en phase finale sur un ordinateur ayant en charge quelques 500 000 abonnés a été estimé à un milliard de caractères au moins. Au moins le tiers des données seront concernées par des traitements en temps réel.
Aucun des calculateurs énumérés plus haut ne permettait d'envisager de tels traitements.
L'intégration progressive de toutes les applications suppose la création d'un support commun pour toutes les informations, une véritable "Banque de données", répartie sur des moyens de traitement nationaux et régionaux, et qui devra rester alimentée, mise à jour en permanence, à partir de la base de l'entreprise, c'est-à-dire les chantiers, les magasins, les guichets des services d'abonnement, les services de personnel etc.
L'étude des différents fichiers à constituer a donc permis de définir les principales caractéristiques du réseau d'ordinateurs nouveaux à mettre en place pour aborder la réalisation du système informatif. L'obligation de faire appel à des ordinateurs de troisième génération, très puissants et dotés de volumineuses mémoires de masse, a conduit à en réduire substantiellement le nombre.
L'implantation de sept centres de calcul interrégionaux constituera un compromis entre : d'une part le désir de réduire le coût économique de l'ensemble, de faciliter la coordination des équipes d'informaticiens; et d'autre part le refus de créer des centres trop importants difficiles à gérer et à diriger,et posant des problèmes délicats de sécurité. Le regroupement des traitements relatifs à plusieurs régions sur chacun de ces sept centres permettra de leur donner une taille relativement homogène. Chaque centre "gérera" environ un million d'abonnés à la fin du VIème Plan.
La mise en place de ces centres a débuté au début de l'année 1971 : un ordinateur IRIS 50 de la Compagnie Internationale pour l'Informatique a été installé à Toulouse en février ; la même machine vient d'être mise en service au centre de calcul interrégional de Bordeaux.

Cela est d'autant plus valable que $T\Delta f$ est plus grand. A cet égard la figure 2 représente la vraie courbe donnant $|\phi(f)|$ en fonction de f pour les valeurs numériques indiquées page précédente.

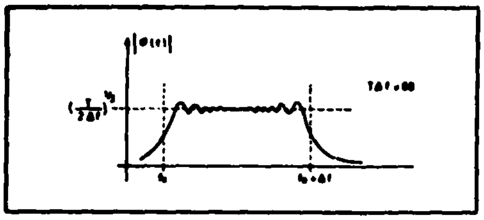


FIG. 2

Dans ce cas, le filtre adapté pourra être constitué, conformément à la figure 3, par la cascade :

— d'un filtre passe-bande de transfert unité pour $f_0 \leq f \leq f_0+\Delta f$ et de transfert quasi nul pour $f < f_0$ et $f > f_0+\Delta f$, filtre ne modifiant pas la phase des composants le traversant ;

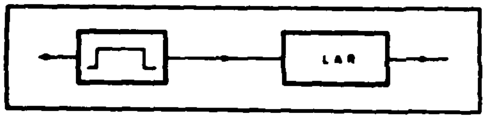


FIG. 3

— filtre suivi d'une ligne à retard (LAR) dispersive ayant un temps de propagation de groupe T_R décroissant linéairement avec la fréquence f suivant l'expression :

$$T_R = T_0+(f_0-f)\,\frac{T}{\Delta f} \quad (\text{avec } T_0 > T)$$

(voir fig. 4).

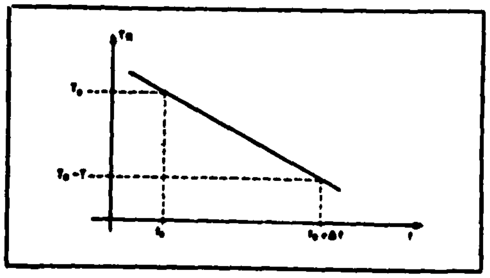


FIG. 4

telle ligne à retard est donnée par :

$$\varphi = -2\pi \int_0^f T_R \, df$$

$$\varphi = -2\pi \left[T_0+\frac{f_0 T}{\Delta f}\right] f + \pi \frac{T}{\Delta f} f^2$$

Et cette phase est bien l'opposé de $\underline{/\phi(f)}$,

à un déphasage constant près (sans importance) et à un retard T_0 près (inévitable).

Un signal utile $S(t)$ traversant un tel filtre adapté donne à la sortie (à un retard T_0 près et à un déphasage près de la porteuse) un signal dont la transformée de Fourier est réelle, constante entre f_0 et $f_0+\Delta f$, et nulle de part et d'autre de f_0 et de $f_0+\Delta f$, c'est-à-dire un signal de fréquence porteuse $f_0+\Delta f/2$ et dont l'enveloppe a la forme indiquée à la figure 5, où l'on a représenté simultanément le signal $S(t)$ et le signal $S_1(t)$ correspondant obtenu à la sortie du filtre adapté. On comprend le nom de récepteur à compression d'impulsion donné à ce genre de filtre adapté : la « largeur » (à 3 dB) du signal comprimé étant égale à $1/\Delta f$, le rapport de compression est de $\frac{T}{1/\Delta f} = T\Delta f$

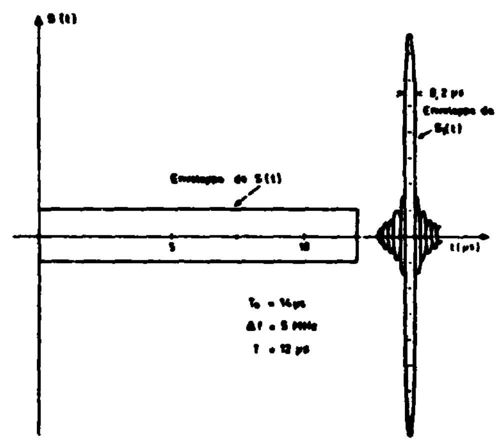
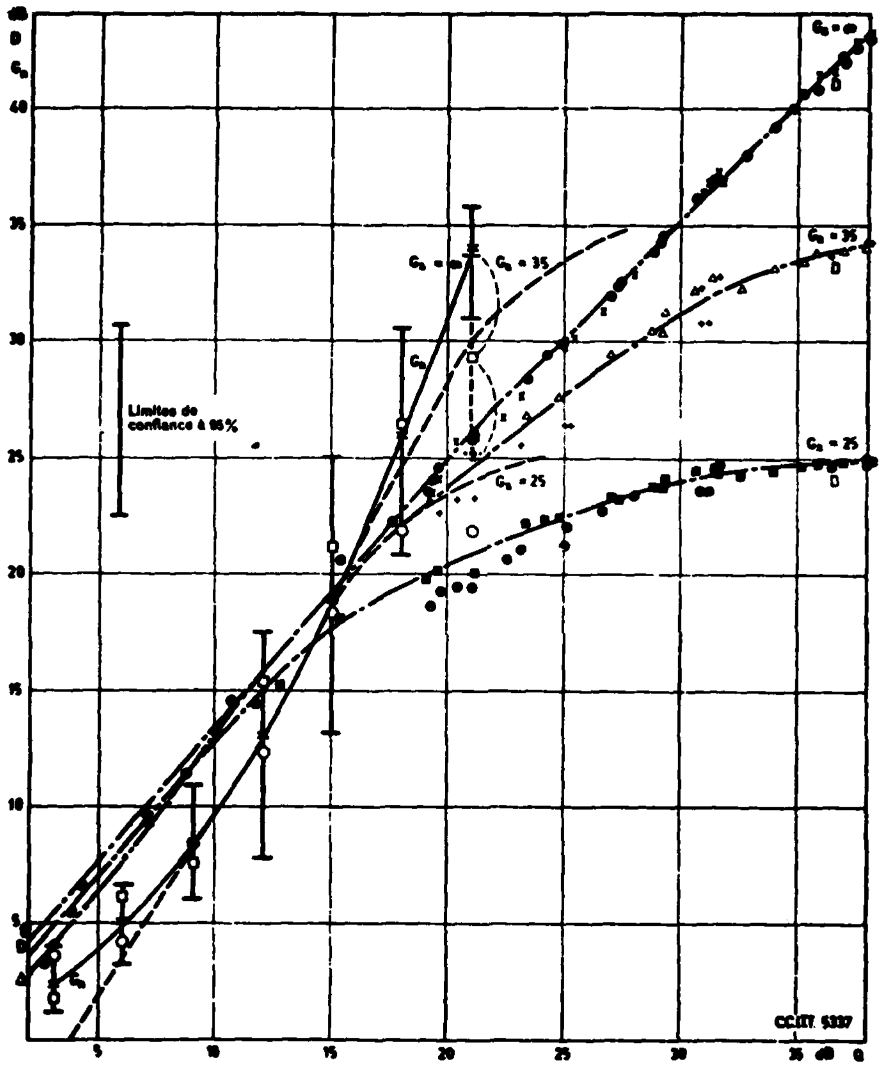


FIG. 5

On saisit physiquement le phénomène de compression en réalisant que lorsque le signal $S(t)$ entre dans la ligne à retard (LAR) la fréquence qui entre la première à l'instant 0 est la fréquence basse f_0, qui met un temps T_0 pour traverser. La fréquence f entre à l'instant $t = (f-f_0)\,\frac{T}{\Delta f}$ et elle met un temps $T_0-(f-f_0)\,\frac{T}{\Delta f}$ pour traverser, ce qui la fait ressortir à l'instant T_0 également. Ainsi donc, le signal $S(t)$



Courbes adaptées G_a (essais subjectifs) pour $G_e = \infty$ $G_e = 35$dB $G_e = 25$dB

[10] ——————— × □ Ω

[23] — — — —

Points calculés $D\,(Q, G_e)$ pour

$G_e = \infty$ $G_e = 25$ $G_e = 35$ dB

● ■ △ – dans la partie montante

× ● + – dans la partie descendante

Courbes —— – ——— – —— $D\,(Q, G_e)$

FIGURE 3

IMAGE 7

CCITTの概要

沿革

CCITTは、国際電気通信連合（ITU）の四つの常設機関（事務総局、国際周波数登録委員会、CCIR、CCITT）の一つとして、ITUの中でも、世界の国際通信上の諸問題を真先に取上げ、その解決方法を見出して行く重要な機関である。日本名は、国際電信電話諮問委員会と称する。

CCITTの前身は、CCIF（国際電話諮問委員会）とCCIT（国際電信諮問委員会）である。CCIFは、1924年にヨーロッパに「国際長距離電話通信諮問委員会」が設置され、これが1925年のパリ電信電話会議のとき、正式に、「国際電話諮問委員会」として万国電信連合の公式機関となったものである。CCITは、同じく1925年の会議のとき、CCIFと併立するものとして設置された。

そして、CCIFは、1956年の12月に第18回総会が開催されたのち、CCITは、同年同月に第8回総会が開催されたのち、併合されて現在のCCITTとなった。このCCITTは、CCIFとCCITが解散した直後、第1回総会を開催し、第2回総会は、1960年にニューデリーで、第3回総会は、1964年、ジュネーブで、第4回総会は、1968年、アルゼンチンで開催された。

CCIFとCCITが合併したのは、有線電気通信の分野、とくに伝送路について電信回線と電話回線とを技術的に分ける意味がなくなってきたこと、各国とも大体において、電信部門と電話部門は同一組織内にあること、CCIFの事務局とCCITの事務局の合併による能率増進等がおもな理由であった。

CCITTは、上述のように、ヨーロッパ内の国ぐにによって、ヨーロッパ内の電信・電話の技術・運用・料金の基準を定め、あるいは統一をはかってきたので、現在でも、その影響を受け、会合参加国は、ヨーロッパの国が多く、ヨーロッパで生起する問題の研究が多い。たとえば、1960年のCCITT勧告の中で、技術上配慮する距離は約2,500kmであったが、これはヨーロッパ内領域を想定したものである。

しかしながら、1956年9月に敷設された大西洋横断電話ケーブルは、大陸間電話通信の自動化および半自動化への技術的可能性を与え、CCITTがこの問題を取り上げるに及び、CCITTの性格は漸次、汎世界的色彩を実質的に帯びるに至った。この汎世界的性格は第2次世界大戦後目ざましくなったアジア・アフリカ植民地の独立に伴ってITUの構成員の中にこれらの国が加わり、ITUの中に新しい意見が導入されたことにも起因して、技術面、政治面の双方から導入されてきた。CCITTの汎世界化は、1960年の第2回総会がニューデリーで開催されたことにもあらわれている。この総会までは、CCIT、CCIFのいずれにしろ、アメリカやアジアで総会が開催されたことがなく、CCITT委員長も、ニューデリー総会の準備文書で、この点には注目すべきであるとのべている。

任務

ITUは、全権委員会議、主管庁会議を始めとして、七つの機関をもち、それぞれの機関の権限と任務は国際電気通信条約に明記されている。そこで条約を参照してみるならば、CCITTの任務は、つぎのとおりとなっている。

「国際電信電話諮問委員会(CCITT)は、電信および電話に関する技術、運用および料金の問題について研究し、および意見を表明することを任務とする。」（1965年モントルー条約第187号）

「各国際諮問委員会は、その任務の進行に当たって、新しい国または発展の途上にある国における地域的および国際的分野にわたる電気通信の創設、発達および改善に直接関連のある問題について研究し、および意見を作成するように妥当な注意を払わなければならない。」（同第188号）

「各国際諮問委員会は、また、関係国の要請に基づき、その国内電気通信の問題について研究し、かつ、勧告を行なうことができる。」（同第189号）

上記第187号と第188号にいわれる「意見」とは、フランス語の Avis から訳したもので、英語では、「勧告（Recommendation）」となっている。CCITTが表明する意見は、国際法的には強制力をもたないものであって、この点が、条約、電信規則、電話規則等各国を拘束する力をもっているものと異なる。もっとも意見とは称しても、技術的分野では、電信規則のごとき、各国政府が承認してその内容を実施する強制規則をもたないので、実際にある機器の仕様を定める場合には、多くの国の意見が統一されたこの「意見」に従わなければ、円滑な国際通信を行なうことができない場合が多い。この意見（または勧告）は、国際通信を行なう場合各国が直面する問題について、具体的意見を表明するもので、たとえば、大陸間ケーブルで大陸間通話を半自動化しようとする場合、その信号方式や取り扱う通話の種類および料金は、どのようにするかを研究して意見を表明する。したがって、CCITTの活動は、つねに時代の最先端を行くもので、CCITTの活動方向は、そのまま世界の国際通信の活動方向であるともいえる。

この意見は、また、電信規則以下のその他の規則のごとく、数年以上の間隔をもって開催される主管庁会議というような大会議の決定をまたなくても表明することができ、また、その改正も容易であるので、現在のように進歩の早い国際通信界では、関係国の意見を統一した国際的見解としては非常に便利である。

memorandum

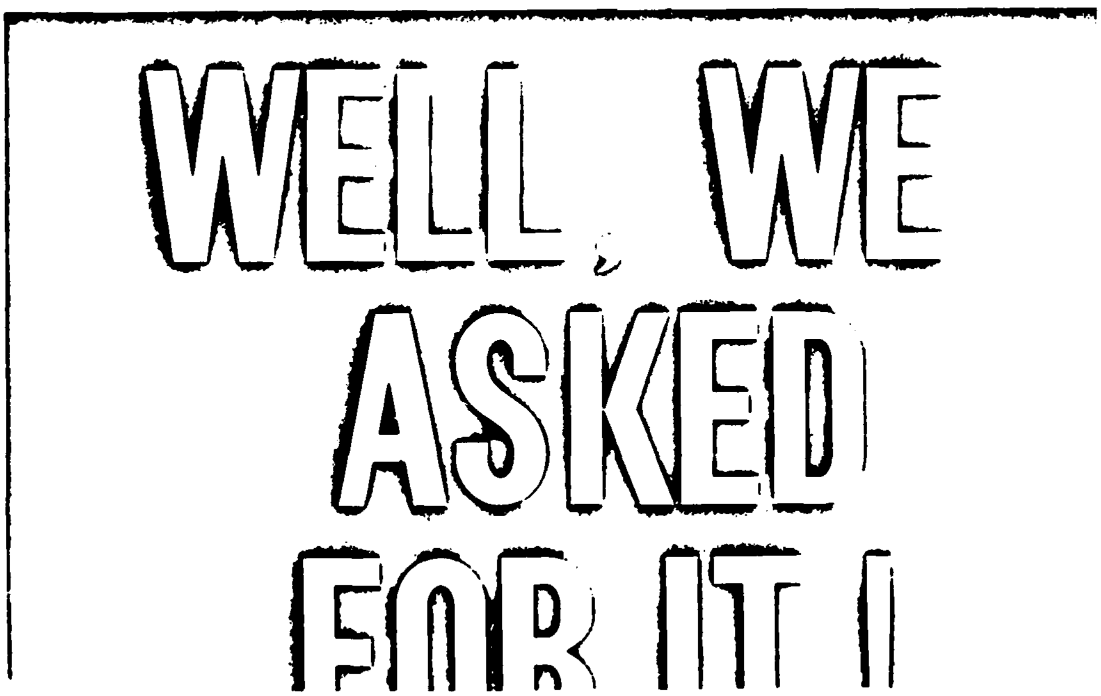
FROM: A.P. Sproggs, Research	TO: G.V. Smith, Project Planning
TEL: EXTN: 2041	DATE: 1-9-71

We know that, where possible, data is reduced to alphanumeric form for transmission by communication systems. However, this can be expensive, and also some data must remain in graphic form. For example, we cannot key-punch an engineering drawing or weather map.

I think we should realise that high speed facsimile transmissions are needed to overcome our problems in efficient graphic data communication. We need research into graphics data compression.

Any comments?

Albert.



2 – BIT			3 – BIT		
Run Length		Code Length	Run Length		Code Length
At Least	But Not More Than		At Least	But Not More Than	
1	2	2	1	4	3
3	6	4	5	8	4
7	14	6	9	16	6
15	30	8	17	32	8
31	62	10	33	64	10
63	126	12	65	128	12
127	254	14	129	256	14
255	510	16	257	512	16
511	1022	18	513	1024	18
1023	2046	20	1025	2048	20

Table A1. Variable-word-length RLC codes with 2-bit minimum and 3-bit minimum length codes.

images with a high percentage of very short runs because of the shorter code length for runs of length 1 and 2.

The fixed-length codes are based upon a repetitive "stacked" pattern with an increase in code length directly proportional to the increase in run length, whereas the variable-length codes increase logarithmically. The 4-bit code is based upon a cycle of 15; ie, the code for a run of 16 is formed by the code for 15 followed by the code for 1. The basic length is 4, with increments of 4 (see table A2).

The 6:3-bit code (table A3) has a basic length of 3 for black and 6 for white, resulting in a cycle of 6 for black and a cycle of 62 for white.

RESULTS AND CONCLUSIONS

Before making any conclusions, it must be noted that the results can be used as representative of bilevel images only. This is due to the variation in compressibility of the different run lengths between algorithms; ie, some algorithms use code lengths proportioned to run lengths while others use longer code lengths for short run lengths. This would create great differences in the effect of some algorithms on presumably noisier lower bit planes in continuous-tone images.

The results of the test are given in table A4. It is obvious that the variable-length codes provide far greater compressibility than the fixed-length codes. The difference is most pronounced for those images which contain the longest runs (ie, images 1 and 2) because the variable-length code lengths are logarithmically and the fixed-length codelengths geometrically related to run length. This result is consistent with previous results, as is the fact that the 4-bit code is substantially better than the 6:3-bit code.

Somewhat unexpectedly, the 75C results compare quite favorably with the variable-length results, at face value. When taking into account the fact that the 75C results also include overhead and the variable-length results do not, the comparison is even more favorable to 75C.

Run Length	Code
1	0000
2	0001
3	0010
4	0011
.	.
.	.
.	.
13	1100
14	1101
15	1110
15	1111
16	11110000
17	11110001
18	11110010

Code Length = 4 x (((run length – 1)/15) + 1)

Table A2. 4-bit fixed-word-length run length code.

Black Runs		White Runs	
Run Length	Code	Run Length	Code
1	000	1	000000
2	001	2	000001
3	010	3	000010
4	011	4	000011
5	100	5	000100
6	101	•	•
6	110	•	•
7	110000	•	•
8	110001	60	111011
9	110010	61	111100
10	110011	62	111101
•	•	62	111110
•	•	63	111110000000
•	•	64	111110000010
•	•	65	111110000011
		•	•
		•	•

Black code length = 3 x ((int(run length – 1)/6)+1)
White code length = 6 x ((int(run length – 1)/62)+1)

Table A3. 6:3-bit fixed-word-length run length code.

	Image 1	Image 2	Image 3	Image 4	Image 5	Image 6	Image 7	Image 8
2-bit variable	13.83	15.30	8.08	4.30	7.26	9.38	4.25	8.69
3-bit variable	14.90	16.07	8.46	4.79	7.68	9.82	4.44	8.91
4-bit fixed	3.39	3.57	3.16	2.59	3.04	3.33	2.66	3.40
6:3-bit fixed	1.92	1.99	1.87	1.66	1.83	1.91	1.64	2.66
75C	12.56	12.50	6.56	4.13	6.11	7.43	3.07	5.58

Table A4. Compression ratios for various algorithms.

RECOMMENDATIONS

USPS has already initiated two contracts for further compression investigations. It is expected that NOSC will follow the progress of these investigations closely.

It is recommended that NOSC increase interaction with other government agencies in order to maintain currency on compression techniques in use. It is also recommended that NOSC make additional effort in the area of encoding simulation. This would be a useful tool for exercising error models for determination of recoverability, as it cannot reasonably be expected that data transmission will be completely error-free. (As an added note, the software impact would be approximately one man-month for each encode-decode combined simulation program required.)

In addition, NOSC should continue to investigate other areas involving data reduction, such as OCR.

APPENDIX B:

IMPROVED TECHNOLOGY EVALUATION

by

Lee A Wise

Code 7323

May 1980

CONTENTS

ILLUSTRATIONS

INTRODUCTION

One of the primary areas of endeavor of project EE25 is the monitoring of the development of the state of the art in image acquisition. This includes not only the imager devices but such things as high-speed clock drivers, widebandwidth amplifiers, track-and-hold amplifiers, analog multiplexers, high-speed analog-to-digital (A/D) converters, and digital data manipulation logic. During the course of this program NOSC has implemented and tested one or more generations of hardware in each of these areas.

As another step in the continuing evaluation of new technology, this report outlines plans for the third-generation scanner testbed to be incorporated in the NOSC Image Capture and Analysis System (ICAS). Also incorporated into ICAS was an 8-bit A/D converter manufactured by TRW, Inc. Preliminary test results on this converter are presented in this report.

PURPOSE

This report provides preliminary test results on a new TRW 8-bit A/D converter and discusses plans for incorporating several new technologies into ICAS during the current fiscal year.

TRW's 8-bit A/D converter will be used to satisfy two purposes in ICAS. First, by using the upper 6 of the 8 bits, this A/D has been shown to produce much better linearity in step sizes than the Phoenix Data 6-bit converters presently in use. This provides not only better image quality but also higher compressibility. Second, with the addition of a new "personality card" designed to accept 8-bit image data and a software set to process 8-bit pels, ICAS will have the complete capability to acquire, process, display, and print 8-bit images.

Another major upgrade to ICAS is the third-generation scanner testbed which is currently in fabrication at NOSC. In mechanical design, the new large drum testbed is very similar to that recently delivered to RCA, Princeton, for use with the time-delay and integration (TDI) imager RCA is developing. The rest of the testbed contains all new designs for illumination source, control electronics, imager clock drivers, analog processing circuitry, and A/D conversion.

TRW 8-BIT A/D CONVERTER

The TRW TDC1007J is a monolithic 8-bit parallel, or flash, A/D converter packaged in a single 64-pin dual in-line package. The device is guaranteed to operate at a 20-megasample-per-second rate but is said to operate typically up to 30 megasamples per second. It is very likely, then, that four of these converters operating in parallel would handle data from a four-channel imager at the full 20-page-per-second rate, which equates to 21 MHz per channel.

A minimum of external circuitry is required to operate this A/D. A very stable voltage reference must be supplied for the resistor divider network, nominally −2.0 volts for a 2-volt full scale analog input range. Also required is an analog input buffer amplifier capable of driving a relatively high capacitive load of 300 pF. Thus, a complete 8-bit A/D can be implemented in a very minimum of circuit board real estate.

TESTING AS A 6-BIT A/D CONVERTER

For initial testing of the TDC 1007J, an evaluation board was purchased which supplies all the required circuitry to begin testing the A/D at relatively low speeds. An interface was designed which allowed the outputs from this A/D to be plug compatible with the existing 6-bit personality card in ICAS. It is this configuration which was used to begin the testing effort, the results of which are presented here.

Figure B1 shows the interface in block form around the TRW evaluation board. The outputs from the interface were wired to allow the upper 6 bits from the 8-bit converter to be used exactly as the 6-bit outputs from 6-bit converters. The two least significant bits were then wired to two unused pins on the output connector to be used by a future personality card designed to make use of all 8 bits. The scanner control signals include the pel clock, line sync, and data available signals. The level decoder and LED display is a very useful aid in setting up the gain and level amplifier to match the dynamic range of the incoming analog signal to the dynamic range of the A/D. A representative layout of the LED display is shown in figure B2. The upper row of LEDs is direct readout of the 8 bits output from the A/D. This display is useful only when calibrating the A/D or otherwise checking performance with near dc voltages input to the unit. The lower row of LEDs decodes the lowest four codes and the highest four codes output from the converter. These outputs are latched so that they remain visible after that particular output code has changed. The latches are all cleared after every sixteenth image line, so that the outputs may accurately track any changes in either the image reflectance or the illumination level falling on the document being scanned.

The initial testing performed on this A/D, used as a 6-bit converter, was accomplished with the procedure described in appendix A of the NOSC fifth annual report, TR 520. The tests described in appendix A were done on the four Phoenix Data 6-bit A/D's. These results may be directly compared to the results presented here for the TRW unit. Figure B3 is reproduced from appendix A of TR 520 and shows the test configuration used for the A/D tests. The Wavetek 175 arbitrary waveform generator is set up to produce a very slowly varying analog ramp voltage spanning the entire input range, which in this case is about 650 mV. The Hewlett-Packard 3455A digital voltmeter is commanded to sample the actual voltage that is input to the A/D. Every time the voltage has changed by 1 mV the MCU is commanded to capture the equivalent of one line of an image. The first pel value is then read from the memory to see what value was output from the A/D. In this way every transition point is recorded for both a positive-going and a negative-going voltage ramp.

The set of analog input voltages corresponding to the actual transition points for each of the 64 output codes was used to plot an actual error characteristic according to the following equation:

$$Y = (X - TA_i) - (TI_i - TA_i - 1/2\ \mathrm{LSB}) \qquad \text{(B-1)}$$

where, for the i^{th} output code,

$$TA_i < X < TA_{i+1}$$

Refer to figure B4 for the definitions of the terms used in equation (B-1). The TI terms are the ideal transition points; eg, TI_1 is the input voltage level at which the transition from output code 0 to output code 1 occurs as the voltage is increased. The TA values are the actual transition points at which the output codes change. The one-half LSB term is equal

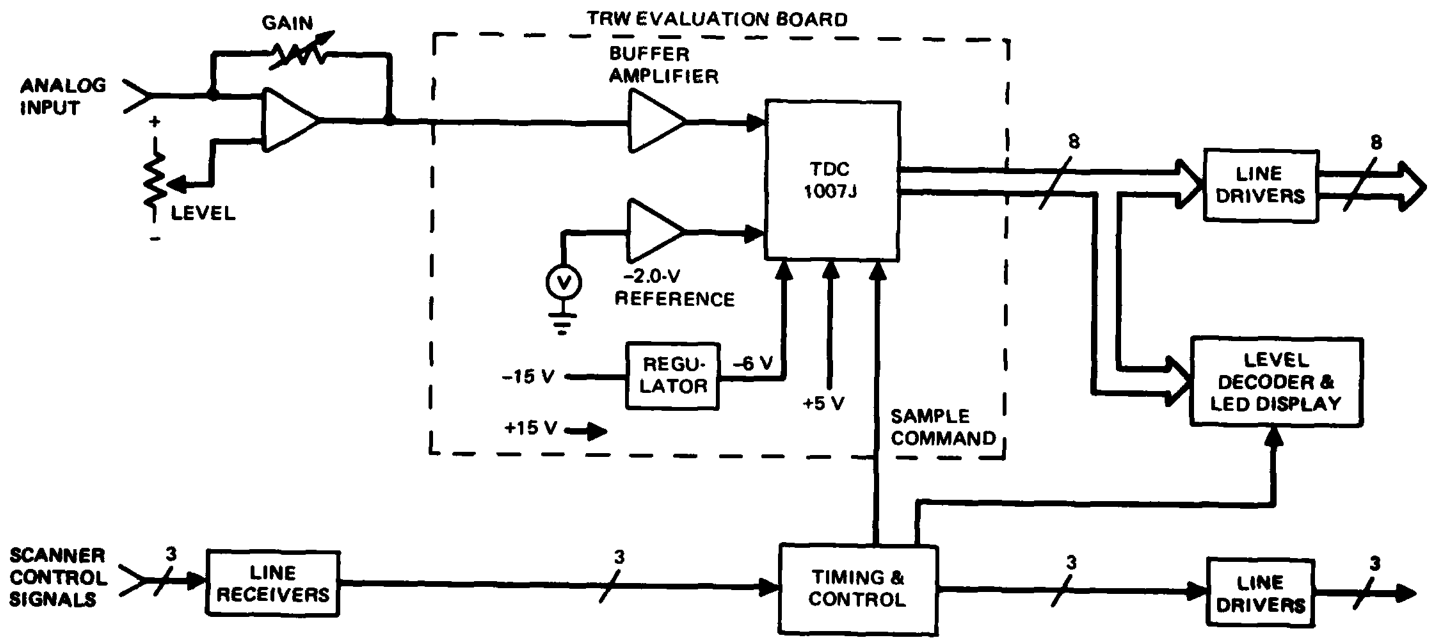


Figure B1. TRW 8-bit A/D converter.

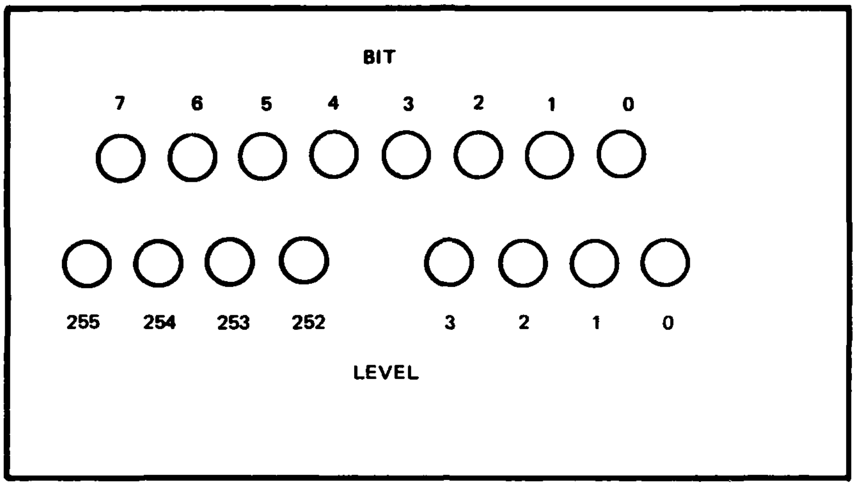


Figure B2. A/D LED display.

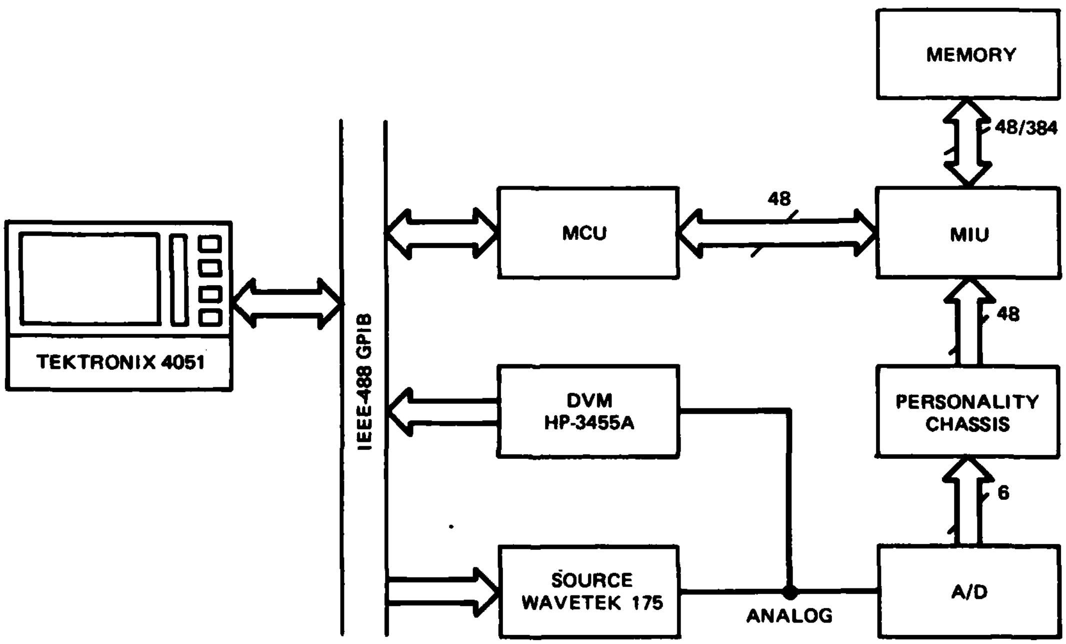


Figure B3. Image Capture and Analysis System (ICAS) test configuration.

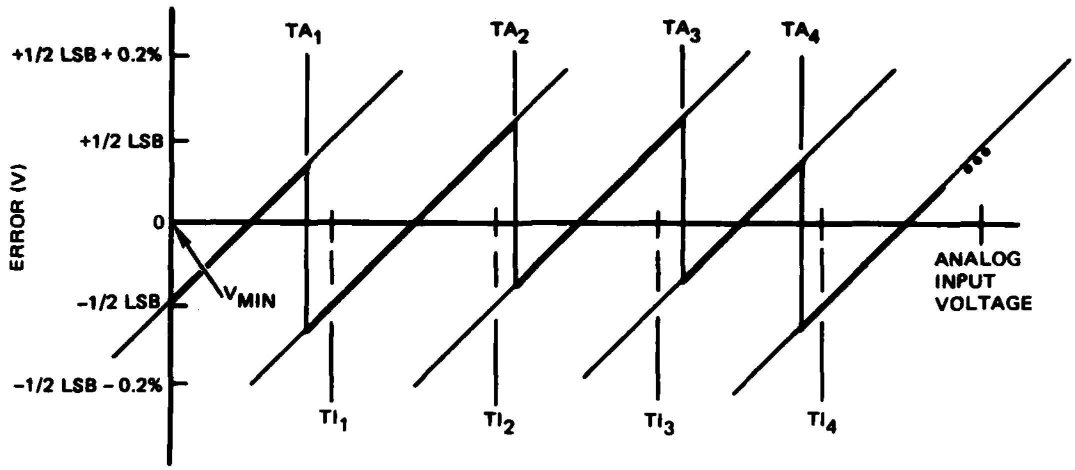


Figure B4. Typical error characteristic.

to one-half an ideal step size expressed in volts. For the A/D in this test, one-half LSB is equal to 4.63 mV. As can be seen in figure B4, the actual error characteristic consists of a series of straight-line segments, each of which passes through zero error at a point exactly midway between the ideal transition points. These points, at zero error, are called the solid code points. To completely specify the error characteristic for the A/D, including the end points, equation (B-1) can be written as follows:

$$Y = X - TI_i - 1/2\ LSB\ ;\ TA_i \leq X \leq TA_i{+}1$$

$$Y = X - Vmin - 1/2\ LSB\ ;\ Vmin \leq X \leq TA_1$$

$$Y = X - TI_{63} - 1/2\ LSB\ ;\ TA_{63} \leq X \leq Vmax$$

where Vmax and Vmin are the upper and lower limits of the analog input range, respectively.

Figures B5 and B6 are the error plots for the A/D for a positive-going ramp and a negative-going ramp, respectively. The linearity specification for this converter is ±1/2 LSB ±0.2% of full scale. With a 600-mV full scale input range the allowable error is ±5.8 mV. The horizontal lines at about ±5.8 mV on figures B5 and B6 indicate the limits of allowable error for the converter. In both figures there is, in general, an offset that if compensated for would come close to eliminating all errors that exceed the limits shown. Also, no account is taken for linearity in the two amplifier stages ahead of the converter, which are a part of the unit under test. This may add a very minor amount to the nonlinearity of the A/D error characteristic.

Upon analyzing the error curves in figures B5 and B6, it is seen that the TRW A/D, used as a 6-bit converter, is superior to the Phoenix Data converter in terms of differential linearity. Refer to the fifth annual report, appendix A, for the details of the Phoenix Data A/D tests. Testing the full 8-bit capability of the converter cannot be done until the 8-bit personality card is completed or until the planned IEEE-488 interface is completed for the new scanner testbed.

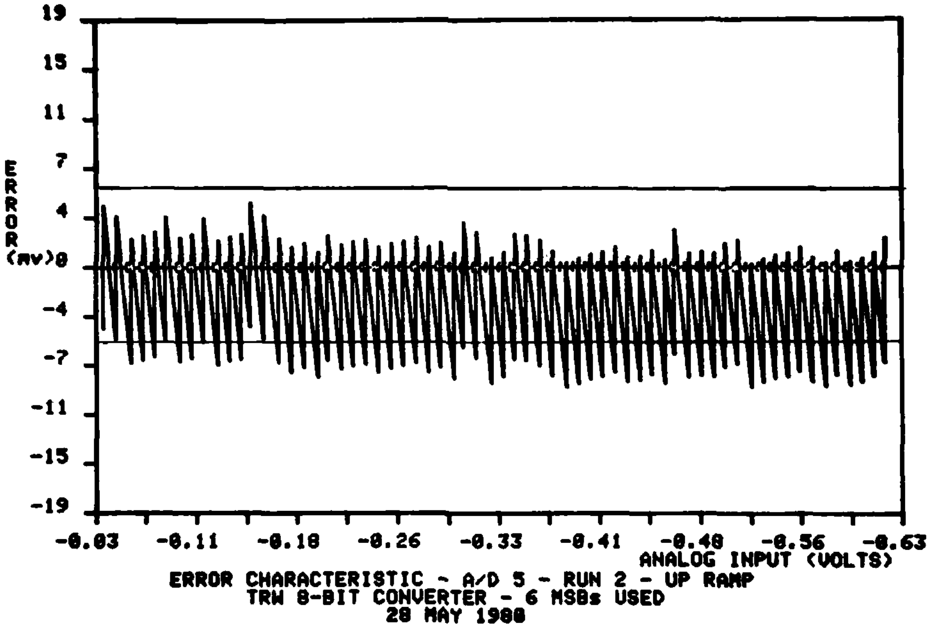


Figure B5. Error characteristic – positive ramp.

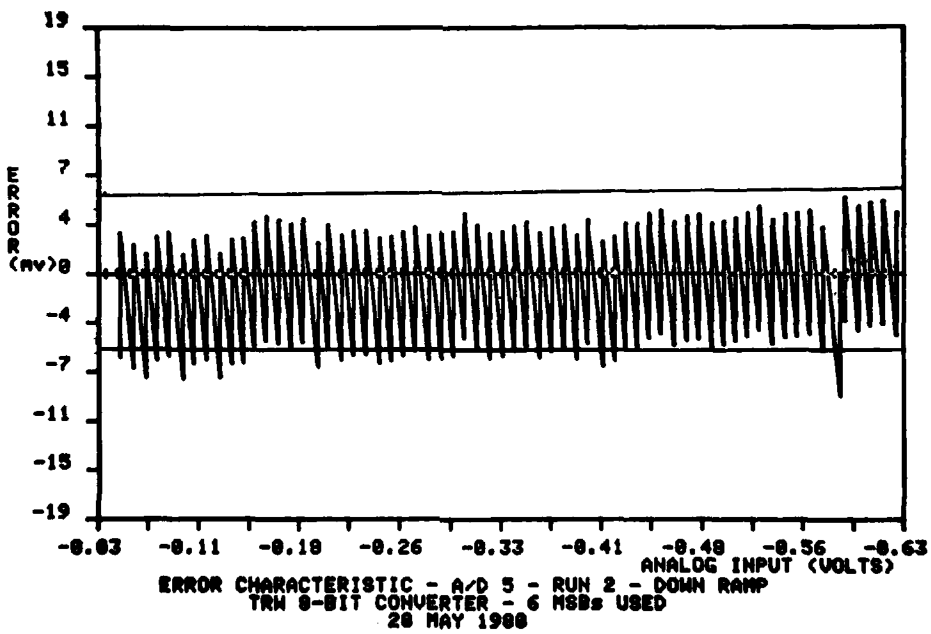


Figure B6. Error characteristic – negative ramp.

Figure B7 shows an illumination profile obtained by using the TRW unit as a 6-bit converter. In comparing this curve with previously reported Phoenix Data converter curves, there are no sharp rises or flat spots in the curve indicative of excessively small or large step sizes. The envelope of the curve in figure B7 is very uniform. This should greatly improve the illumination correction procedure by eliminating the degradation of compressibility of the images, experienced in the past. The photograph in figure B8 is the first example of an image digitized with the new A/D and corrected with the illumination profile of figure B7. The resultant printed image does appear to be darker in general than the original document. This is because no detailed calibration of the D/A and video amplifier has been performed as of this date.

PLANNED 8-BIT IMAGE PROCESSING CAPABILITY

With the increased intensity resolution capability of the 8-bit A/D converter it is very desirable not only to investigate 8-bit images but also to investigate higher accuracy in processing 8-bit images to obtain improved 6-bit or 1-bit (thresholded) images. The following items are currently in progress to provide this much needed capability in ICAS.

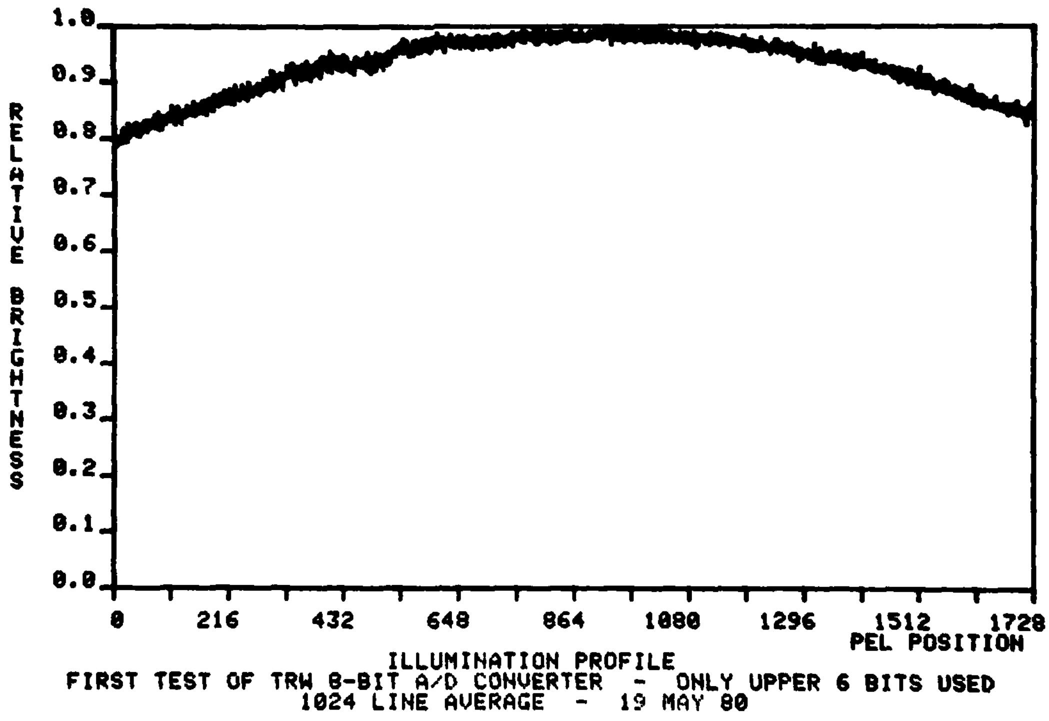


Figure B7. Illumination profile.

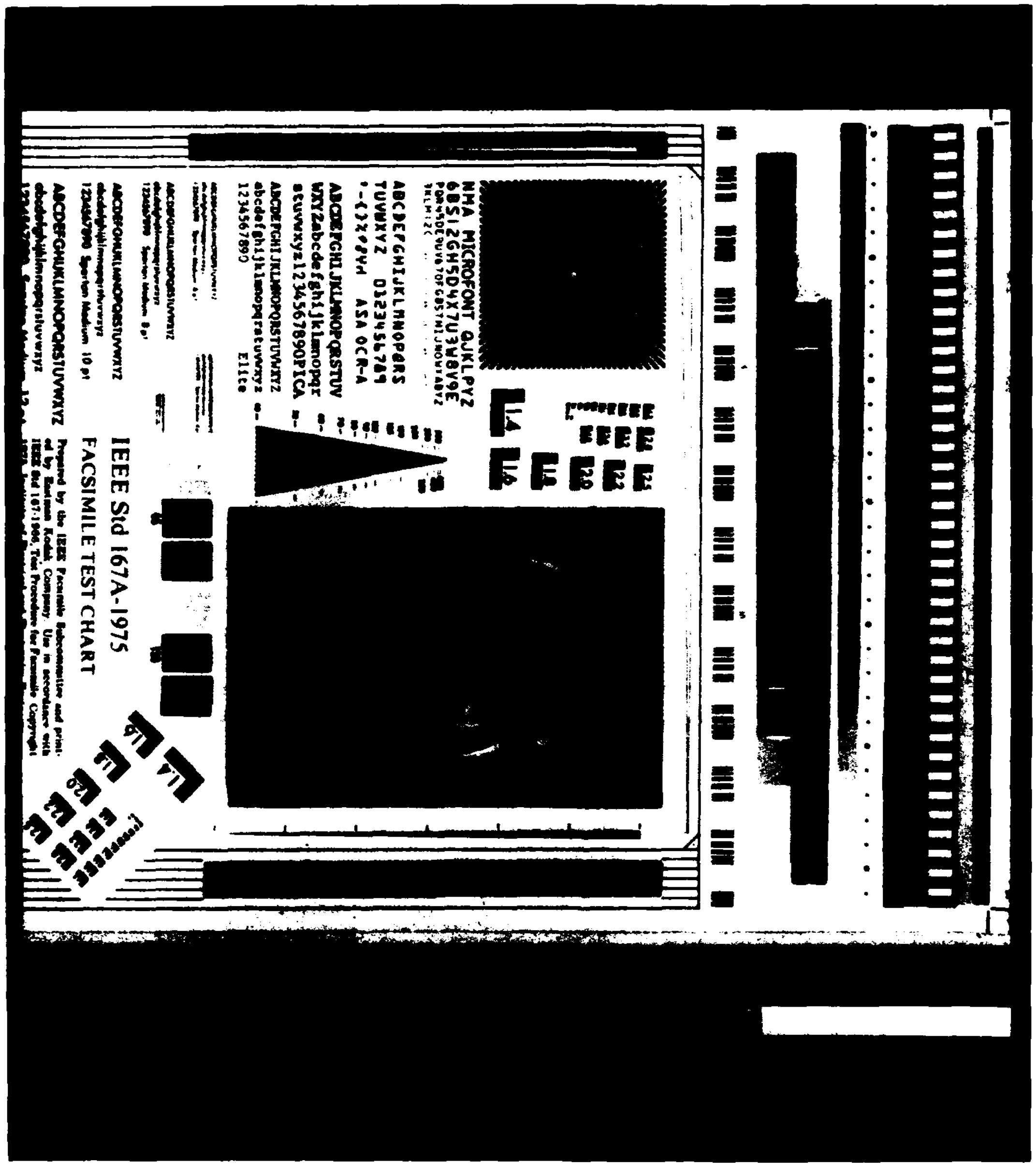


Figure B8. IEEE facsimile test chart.

8-BIT PERSONALITY CARD

A new single-channel personality card is currently in design which will have the capability of formatting 8-bit pels for storage into the 48-bit frame-store memory (FSM). This same card will also be switchable to provide formatting 6-bit pels into 48-bit words for capturing 6-bit images, as the present personality card does.

In order to accommodate the required circuitry to perform these functions, it was necessary to purchase a new wire-wrap card design from Augat, Inc. This new design contains integrated circuit (IC) locations for ECL/TTL translators and a universal pin pattern for Schottky TTL circuits, as opposed to the earlier design containing 16-pin patterns for all IC locations. The universal pattern allows the use of ICs with more than 16 pins. For this personality card it is necessary to use 20-pin ICs containing 8-bit latches in order to get all the required functions on one card. This new card design will likely be added to Augat's standard product line.

DISPLAY OF 8-BIT IMAGES

The display hardware in the MIU which drives the Conrac B/W Monitor is capable of displaying only 6-bit image data that are organized in memory as 6-bit pels. It would be possible to design a new display card to utilize 6- and 8-bit pels, but the Comtal Display System is available to be used to display all 8-bit images for the present time. With the Comtal display, up to a 512-by-512-pel image segment must be transferred from the FSM to the Comtal unit for display. With this configuration, the capability for roaming over the entire image in the FSM is lost. The image must be examined one 512-by-512 segment at a time. However, once the 8-bit image is written onto tape, it can easily be read back from tape, and stored in the FSM as 6-bit pels, allowing the original display versatility of the ICAS, albeit at a 6-bit resolution. This will still be very useful for checking image integrity before or after various processing functions.

ICAS SOFTWARE UPGRADES

The ICAS software is currently being modified to allow the acquisition, display, analysis, and other processing of 8-bit as well as 6-bit images. No major algorithm changes are involved. However, the programs must be modified to operate with a specific set of constants which will be interchangeable for 6-bit and 8-bit processing. Some of the software modules to be modified are the following, in prioritized order:

MCU/Comtal data transfer package. This includes not only image data transfers, but also function table and pseudocolor table data transfers.

Illumination correction. The basic correction algorithm will not be changed, but a new program will be written to generate the output pel value look-up table for 8-bit correction.

Statistical analysis. This includes pel brightness, first difference, spatial frequency, and run length statistics.

Compressibility calculations. These include compressibility calculations for four run length codes plus the proprietary 75C algorithm compression and decompression software.

THIRD-GENERATION SCANNER TESTBED

NOSC recently fabricated and delivered a large drum test bed (LDTB) to RCA, Princeton, for use in testing the new TDI imagers as they are fabricated. The test electronics supplied with the previous imager, under an earlier contract with RCA, were physically too large to be mounted on the current LDTB at NOSC since the optical axis is only 2 inches above the table surface. The new LDTB just delivered to RCA has the optical axis 7 inches above the table. In order for NOSC to be compatible with the RCA LDTB, modifications were considered for the current table. At the same time consideration was given to a better illumination source. This resulted in a contract to Fairchild, Syosset, for an illumination source built to their latest design, which is similar to the USPS EDM scanner. The end result of these and other considerations is that a completely new scanner testbed is being fabricated which will have much more capability and versatility than the earlier LDTB. Photographs of the LDTB delivered to RCA are shown in figure B9.

SCANNER III

A sketch of the new third-generation scanner equipment is shown in figure B10. The scanner table and drum will very closely resemble the one shown in figure B9 with the exception of the illumination source. As mentioned, a contract has been let to Fairchild, Syosset, for a new illumination source utilizing 24-inch fluorescent tubes. It is expected that this will greatly improve the uniformity of illumination across the drum surface. Also of concern is the aging process in the tubes themselves. The NOSC source is driven by dc voltage with the polarity reversed on a daily basis, whereas the Fairchild system used a 19-kHz ac voltage.

Below the scanner table is a new rollabout cart which has two 19-inch rack-mount sections to accommodate all the LDTB electronics, power supplies, and motor controls.

The current LDTB at NOSC has the electronics housed in an enclosure mounted above the optical axis and the power supplies mounted underneath the table between the side rails. This layout does not provide convenient access for the power supplies at all, especially in view of the fact that the new table is going to be larger than the old one. The new cart will provide much better access to the power supplies. It will also allow a more reasonable packaging scheme for the digital and analog ciruitry associated with the new scanner. It is further expected that the same card cage may be used with the TDI imagers by only exchanging digital and analog card sets.

Figure B9. New large drum test bed.

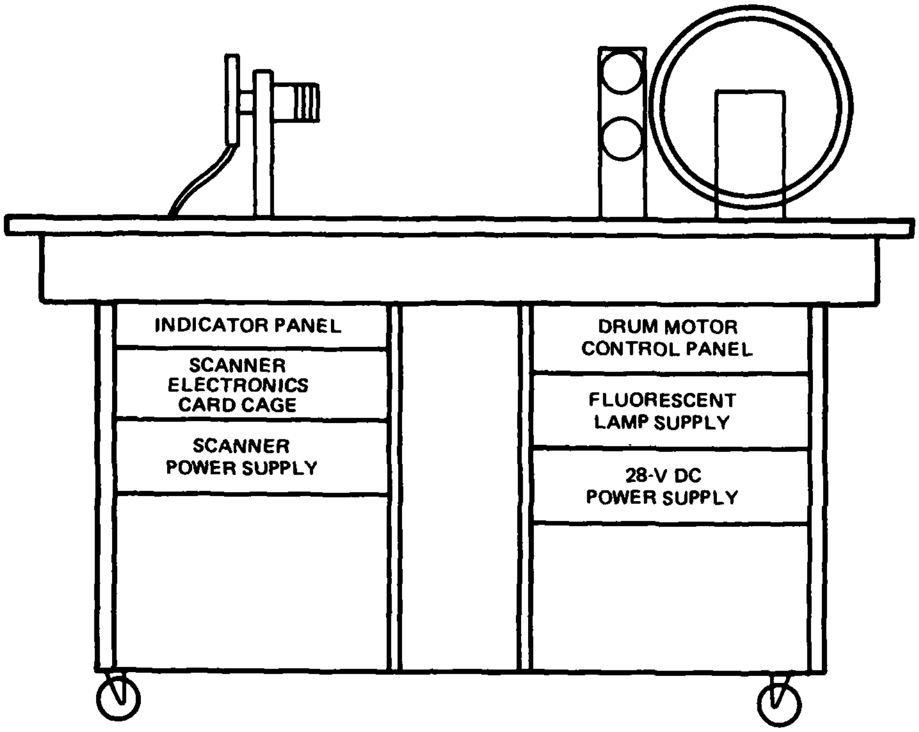


Figure 10. Scanner III.

PLANNED IMAGER ACCOMMODATION

The latest-generation CCD imager (linear) is the Fairchild CCD143, a 2048-element imager specified to have increased sensitivity in the blue region to the spectrum. This is the same device that Fairchild, Syosset, has proposed for use in the USPS engineering model (EM) scanner. The device is also specified to operate up to about 20 megapels per second.

Also, as mentioned, it is planned to test the new TDI imagers developed by RCA, Princeton. The new scanner table with the optical axis 7 inches off the table surface should easily accommodate the device and its driver electronics.

IMAGER DRIVER ELECTRONICS

One of the main areas of concern in operating CCD imagers at very high speeds is the clock driver circuitry. The new design linear imager, the CCD143, has incorporated on-chip clock drivers which generate the different phases of clocks required to shift data out of the device. However, the one transport clock that is required does present a fairly high capacitive load to the clock driver of about 700 pF. This type of load requires the clock driver to be able to dissipate about 3 watts of average power and supply peak currents of over 0.5 ampere when operating at 10 MHz. With careful packaging it is felt that the DS0056 clock driver will handle this task.

Of more concern are the requirements of the RCA TDI imager. The preliminary specifications obtained to date indicate that one or more clock inputs present about 1000-pF loads to the clock driver and are designed to operate at 21-25 MHz. The clock rise and fall times are also to be less than 20 nanoseconds. To meet these requirements, the clock driver must be able to supply 1.5-ampere peak currents and must dissipate about 7 watts. This is definitely beyond the capability of all known IC clock driver circuits on the market. NOSC is beginning an investigation into the design of discrete element clock drivers. The designs currently in fabrication utilize vertical metal-oxide-semiconductor field-effect transistors (VMOS power FETs).

ANALOG PROCESSING

The planned analog processing circuitry is shown in block diagram form in figure B11 for the new CCD143 imager. Unlike the CCD121H NOSC is presently using, which has an on-chip analog multiplexer, the CCD143 contains two analog output ports. It is planned to house all the analog processing circuitry on the imager driver board and the analog processing board which will be in the scanner electronics card cage (figure B10). This design eliminates one long transmission path that previously existed from the scanner to the gain/level and A/D chassis. With the signal transmission paths kept to a minimum the signal quality will not be affected as much as with the previous system.

DIGITAL CONTROL

With the requirement of 8-bit image processing or with the possible increased spatial resolution up to 300 by 300 pels per inch, it will no longer be possible to store complete 8 1/2-by-11-inch images in the NOSC FSM. It is therefore desirable to be able to easily scan portions of an image at a time and to logically "tile" these segments together and store them as a single contiguous image on tape. To do this, the digital control electronics has been redesigned to allow various image parameters to be set up via the general purpose interface bus (GPIB). With the development of essentially a single-chip interface circuit for the GPIB, this becomes an easy task.

The control electronics will allow various parameters to be entered into a set of control registers before each capture, such as:

number of lines delayed after drum sync

number of lines to be captured

number of pels delayed on each line

number of pels per line to be captured

This interface also allows the capture command to be sent automatically to the scanner to provide digital control of the scanner. Previous operation required several manual pushbutton operations to initiate each capture sequence.

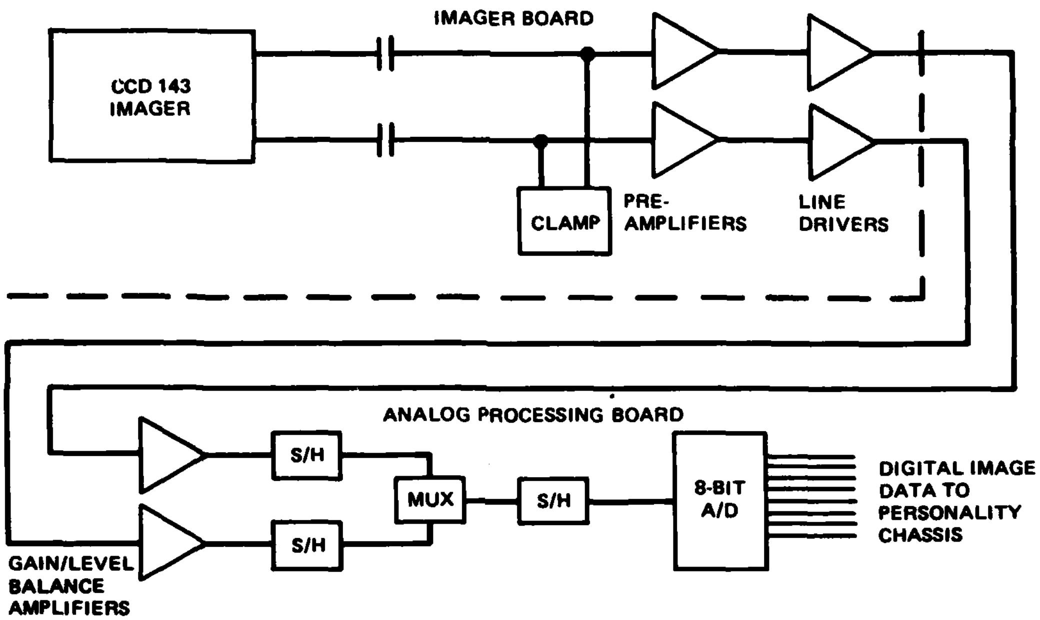


Figure B11. Simplified block diagram.

HARDWARE ILLUMINATION CORRECTION AND EDGE ENHANCEMENT

NOSC has awarded a contract to Data/Ware Development, Inc in San Diego to design and fabricate hardware capable of performing illumination correction and edge enhancement at the full 20-page-per-second rate, based on four channels operating in parallel at 21 MHz each. The first phase of the contract calls for delivery of a single-channel system in early 1981. This will accommodate the maximum data rate possible from the CCD143 imager. The unique design approach utilizes the latest technology in high-speed RAM and Schottky TTL circuitry.

RESULTS AND CONCLUSIONS

On the basis of preliminary testing performed on the TRW 8-bit A/D converter, it has been shown to be superior to the Phoenix Data 6-bit A/D when used as a 6-bit converter. Since this A/D is a single monolithic IC design, it can be packaged on the same circuit board as all the analog processing circuitry, eliminating one data transmission path.

Two additional A/D chips will be purchased, providing for a complete four-channel 6-bit A/D capability in preparation for testing the RCA TDI imagers.

PLANNED FUTURE ACTIVITIES

1. Proceed with the conversion of ICAS software to provide compatibility with both 6-bit and 8-bit image data.

2. Complete designs for and fabricate:

   a. 6-bit/8-bit personality card for a single-channel imager

   b. Scanner III testbed

   c. CCD143 driver electronics

   d. CCD143 analog processing circuitry

   e. Scanner digital control electronics

3. Continue investigation of very high-speed clock driver circuits in preparation for testing RCA TDI imager at full speed.

4. Begin full 8-bit characterization of TRW 8-bit A/D converters.

5. Begin characterization of CCD143 imager.

6. As data become available, begin plans for testing the RCA TDI imagers.

APPENDIX C:

DATA CAPTURE

by

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Code 7132

Ronald J Wagar

Code 7323

May 1980

CONTENTS

ILLUSTRATIONS

TABLES

OBJECTIVES

The objective of this NOSC/USPS program task is to formulate algorithmic procedures for high-speed automatic classification of documents presented to input stations of the Electronic Message Service System (EMSS). The document classification algorithms are based on the set of statistical image measures developed under the FY78 NOSC/USPS program to characterize the properties of typewritten, continuous-tone, and other image data types.

The major goal of the current task is to recognize with a high degree of confidence those documents which contain only bilevel (black/white facsimile) information. Threshold digitization of such documents offers at least a factor of six improvement in compressibility over digitized continuous-tone documents. Further, if it can be determined that a document is in a form suitable for processing by optical character recognition (OCR) equipment, the compressibility improvement over a digitized continuous-tone document can be as high as 1500 to 1. Since the statistical mix of EMSS input documents is expected to be rich in typed business correspondence, the payoff for accurately identifying and properly compressing this type of input document is potentially very high.

A closely related objective is the classification of document segments. Of particular interest is the localization of signature blocks which could be scanned, digitized, compressed, and transmitted in a special format while the remaining document text is processed by OCR techniques. Also, the identification of logo areas acceptable for OCR processing could be exploited to achieve additional gains in image compressibility.

A final objective is that all image-type classification algorithms developed be easily replaceable by high-speed hardware/software modules capable of operating at the required EMSS real-time document acceptance rates.

BACKGROUND

The sequence of operations for EMSS input document digitization, classification, compression, and transmission is shown in the data flow diagram of figure C1. Input documents are digitized by scanning at 6 (or 8)-bit resolution at each picture element (pel) location. Selected image statistical measures are compiled for each scanned document and used for image-type classification. Documents classified as being typewritten text are transferred directly to the OCR processor for conversion to USASCII format.

Typewritten text or similar documents deemed unacceptable for OCR processing are subjected to bilevel thresholding for conversion into a binary bit stream. Additional compaction procedures can be applied to the bit stream prior to data transmission. Documents classified as continuous-tone images are processed directly by continuous-tone data compression equipment. The image data are compacted by using optimum MSE or other error minimization criteria to efficiently encode the continuous-tone image data for minimum bandwidth transmission.

Three principal statistical image measures useful for image-type classification were developed under the FY78 NOSC/USPS program (ref 1). These image statistics are the pel brightness sums resulting from vertical and horizontal image scans (denoted SFI_v and SFI_h, respectively) and the frequency histogram of the pel brightness levels (termed PBS). As part of this effort, a data base of test images was assembled. The data base test images were grouped into approximately 15 categories and included examples of typewritten and

1. Advanced Mail Systems Scanner Technology Fourth Annual Report, NOSC TR 358, October 1978.

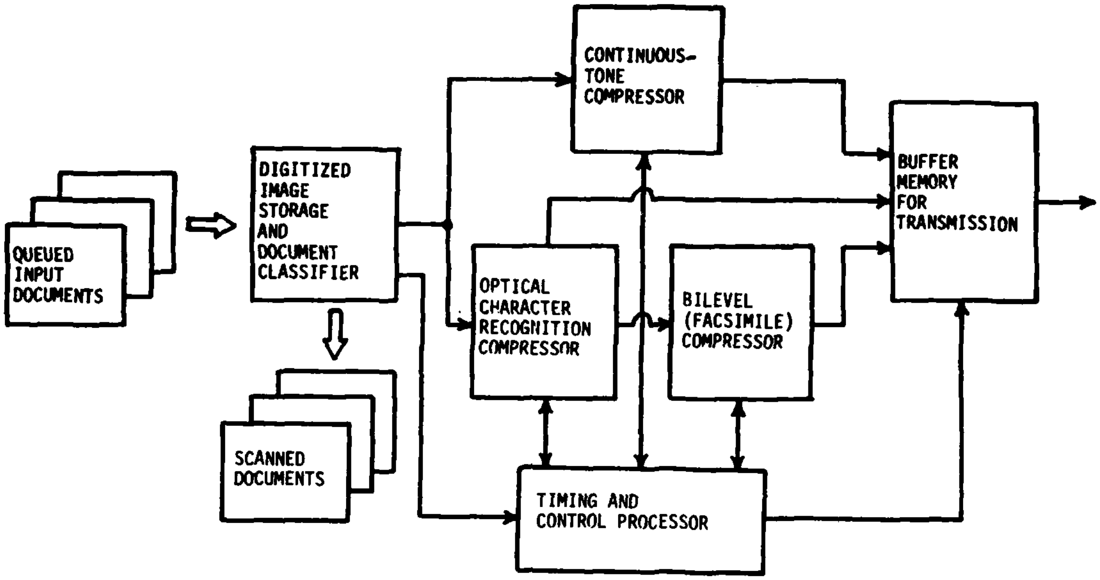

Figure C1. EMSS document and digitized data flow diagram.

handwritten pages, continuous-tone images, preprinted forms, and other commonly occurring image types.

By using the three principal image statistics, selected images from the data base were classified as to their suitability for either binary thresholding (for OCR) or 6-bit resolution coding. This classification was performed by subjective evaluation of the computed statistics for each image tested. The results obtained with the 21 data base test images are shown in table C1 and indicate that correct classifications as to image coding requirements could be made for 19 of these images. Further, a close examination of the cases in which incorrect classifications had been made – ie, requiring 6-bit resolution coding of typewritten pages – indicated that the major contributing factor was low print contrast ratios. In these instances, the choice of 6-bit coding for the typewritten images was probably the appropriate one.

Based on the encouraging results of subjectively classifying the data base test images by using the three statistical image measures, emphasis has now shifted to the definition of algorithms for performing image classification in an automatic fashion. The remainder of this report discusses the development and preliminary evaluation of a set of automatic image-type classification algorithms.

Document No	Class and Type	SFi_v	SFI_h	PBS	Decision	Correct
02-01	Typed Page, Unsigned, No Logo	Yes	Yes	BL	THR (OCR?)	Yes
02-02	Typed Page, Unsigned, No Logo	Yes	Yes	BL	THR (OCR?)	Yes
03-01	Typed Page, Unsigned, B/W Logo	Yes	Yes	BL	THR (OCR?)	Yes
03-02	Typed Page, Unsigned, B/W Logo	Yes	Yes	BL	THR (OCR?)	Yes
04-01	Typed Page, Unsigned, Color Logo	Yes	No	ML	Cont Tone	Yes
04-02	Typed Page, Unsigned, Color Logo	Yes	Yes	BL	THR (OCR?)	Yes
06-01	Handwritten (ink)	Yes	No	BL	Cont Tone	Yes
11-01	B/W Photo, Circuit Board	No*	No*	ML	Cont Tone	Yes
13-01	Image Standards, Fax Chart	No*	No*	ML	Cont Tone	Yes
14-01	Form, Blank (Green)	No	No	BL	Cont Tone	Yes
15-01	Form, Completed (Red Stamp)	No	No	BL*	Cont Tone	Yes
16-01	Eng Drawings, Versatec Plot	No	No	BL*	Cont Tone	Yes
17-01	Circulars (Newswk Ad) Multicolor	Yes	No	ML*	Cont Tone	Yes
0(148)	Fairchild Letter	Yes	Yes	BL	THR (OCR?)	Yes
0(148)	Fairchild Letter, Corrected	Yes	Yes	BL	THR (OCR?)	Yes
0(456)	Fairchild Letter	Yes	Yes	BL	THR (OCR?)	Yes
0(456)	Fairchild Letter, Corrected	Yes	Yes	BL	THR (OCR?)	Yes
0(820)	Fairchild Letter	Yes	Yes	BL*	THR (OCR?)	Yes
0(820)	Fairchild Letter, Corrected	Yes	Yes	BL	THR (OCR?)	Yes
0(1208)	Fairchild Letter	Yes	No	BL	Cont Tone	$\boxed{\text{No}}$
0(1208)	Fairchild Letter, Corrected	Yes	No	BL*	Cont Tone	$\boxed{\text{No}}$

Table C1. Image classification summary.

APPROACH

DOCUMENT ANALYSIS

For the purpose of performing a preliminary analysis of automatic image-type classification, a data set of typewritten images was generated. The data set consists of 12 examples of typewritten text in which the three parameters of characters per inch, line spacing, and right margin justification are varied. Two different horizontal character spacings were used, 10 pitch and 12 pitch. Similarly, single, space-and-a-half, and double line spacing are considered. Finally, the presence or absence of right margin justification was included, resulting in the 12 typewritten test images. Two additional images included in the data set are a continuous-tone photograph of a circuit board and the standard IEEE facsimile test chart.

Four images representative of both image types were scanned at a spatial resolution of 200 by 200 pels per inch for algorithm evaluation purposes. Two of the selected images are typewritten text examples and are characterized as 12 pitch, single space, with and without right margin justification. It should be noted that the Wang model 5581 Daisy Printer used to generate the typewritten text examples employs noninteger horizontal character spacing when performing right margin justification. Thus, there is a significant reduction in columnwise character alignment in this output mode. This fact has significant implications for image-type classification based on the horizontal pel brightness sum measure, SFI_h. The typewritten text examples and their SFI_v, SFI_h, and PBS statistics are shown in figures C2 through C9, respectively. The remaining two images selected for evaluation are the photograph of the circuit board and the IEEE facsimile test chart. These images and their respective statistics are given in figures C10 through C17.

PROPERTIES OF STATISTICAL IMAGE MEASURES

VERTICAL BRIGHTNESS SUM

The vertical pel brightness sum image statistic, SFI_v, is the cumulative brightness of each line of a scanned image. It is obtained by summing the individual pel brightness values along a line. An example of the SFI_v statistic is shown in figure C18. This figure indicates the presence of two distinct spatial frequency components in the SFI_v statistic. The first, denoted F_1, corresponds to the vertical spacing between lines of typewritten text. The second, F_2, is related to the horizontal line structure spacing within the characters on a line. Of these, F_1 is the dominant component and is the image statistic property for which image-type classification information can principally be derived.

The periodic structure of the SFI_v statistic reflects the repetitive line spacing structure inherent in a typewritten page. Photographic continuous-tone images do not, in general, exhibit strong repetitive features in the SFI_v statistic. However, the continuous-tone circuit board image of figure C10 is an example of a photographic image in which repeating structures are present. The implication of this figure is that additional processing of the SFI_v statistic is required to determine whether the spatial frequency of the repeating structure is consistent with the spatial frequencies of standard typewritten text line spacings.

10 April 1980
467A

Mr. W. T. Marable, Executive Director
Research & Development Laboratories
11711 Parklawn Avenue
Rockville, Maryland 20852

Gentlemen:

This is a sample of a letter we use as a "standard" for imaging experiments at NOSC, San Diego. It was made on a Wang Word Processor 30, and printed with a Wang Model 5581 Daisy Printer. The keystroke information is recorded on a 10 megabyte sealed disk in United States of America Standard Code for Information Interchange (USASCII) format. This is a standard seven-bit (plus parity) binary code for each keystroke which is widely used in industry. In USASCII form, this page as written can be exactly defined by 1777 characters (14216 bits) of data (excluding signature, logo, or header information). When scanned at 200-by-200 picture elements per inch with six bits per element for grey scale, the page is defined by 22,440,000 bits.

By recording this letter on the hard disk (and/or on the archive single diskette), it is possible to reproduce a quantity of duplicate originals, all nominally identical. Since the printer is a modified Xerox Diablo typewriter, it is also possible to change ribbons (a five-minute process) to yield copies of differing colors. It is of course possible to write on all textures, colors and weights of paper with or without letter head. It will also allow copies of this text to be analyzed both with and without signatures of various colors.

This ability to provide complete parameter selection and consistency control for analysis of thresholds, contrasts, color separation, compressibility coefficients, and character fonts will be of great benefit in quantifying the requirements of U. S. Postal Service scanner technology.

Frank Martin
NOSC Code 7323
Problem EE25

Figure C2. Typewritten text – 12 pitch, single space, without right margin justification.

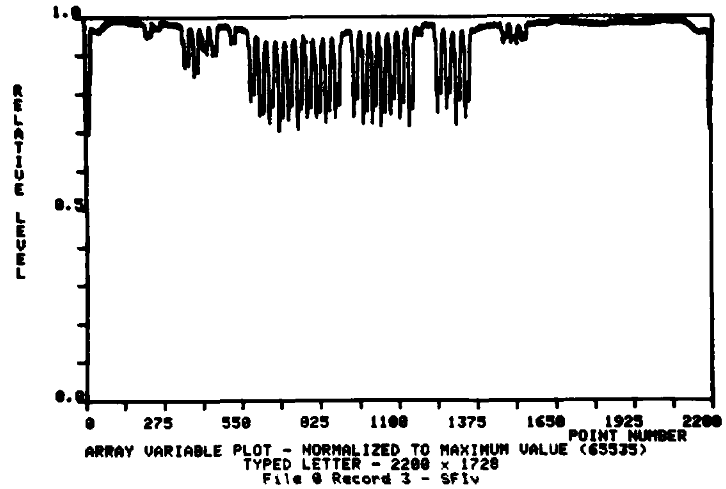

Figure C3. Typewritten text – vertical brightness sum (SFI_v).

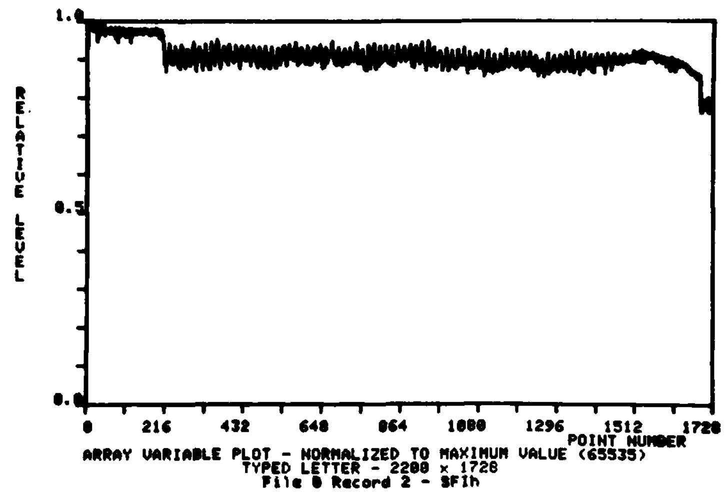

Figure C4. Typewritten text – horizontal brightness sum (SFI_h).

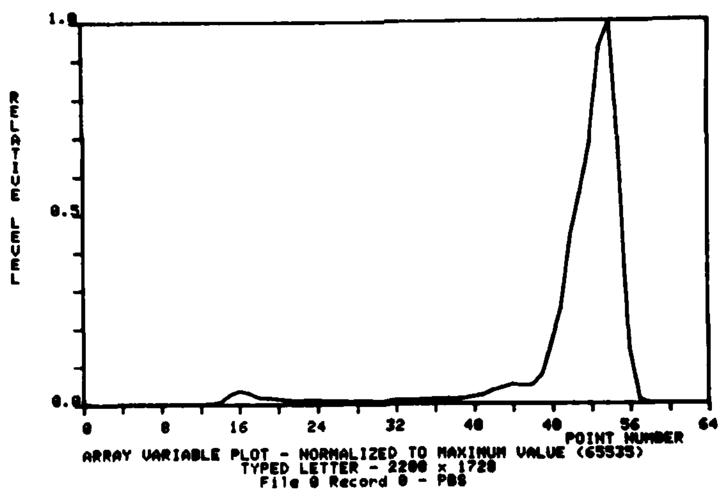

Figure C5. Typewritten text – pel brightness histogram (PBS).

10 April 1980
467A

Mr. W. T. Marable, Executive Director
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This ability to provide complete parameter selection and consistency control for analysis of thresholds, contrasts, color separation, compressibility coefficients, and character fonts will be of great benefit in quantifying the requirements of U. S. Postal Service scanner technology.

Frank Martin
NOSC Code 7323
Problem EE25

Figure C6. Typewritten text – 12 pitch, single space, with right margin justification.

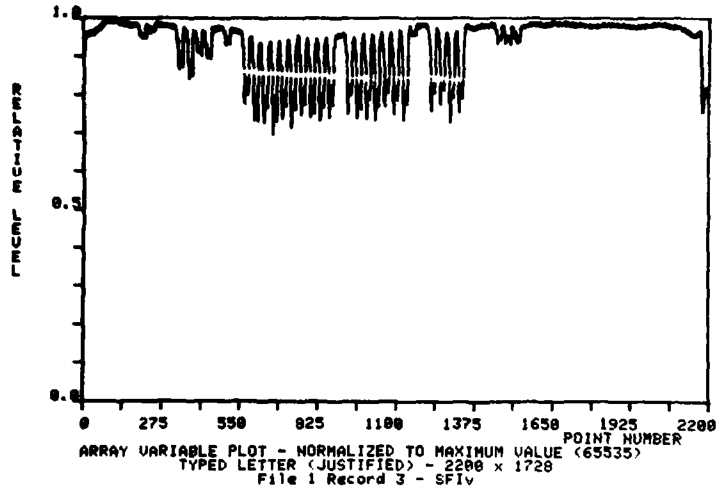


Figure C7. Typewritten text – vertical brightness sum (SFI_v).

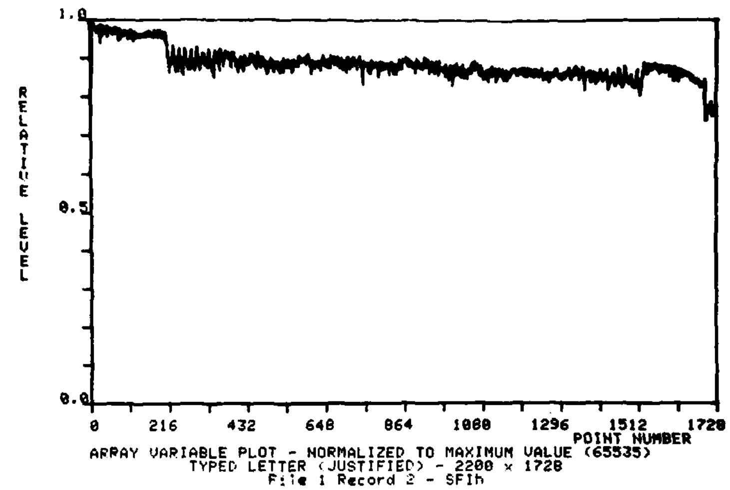


Figure C8. Typewritten text – horizontal brightness sum (SFI_h).

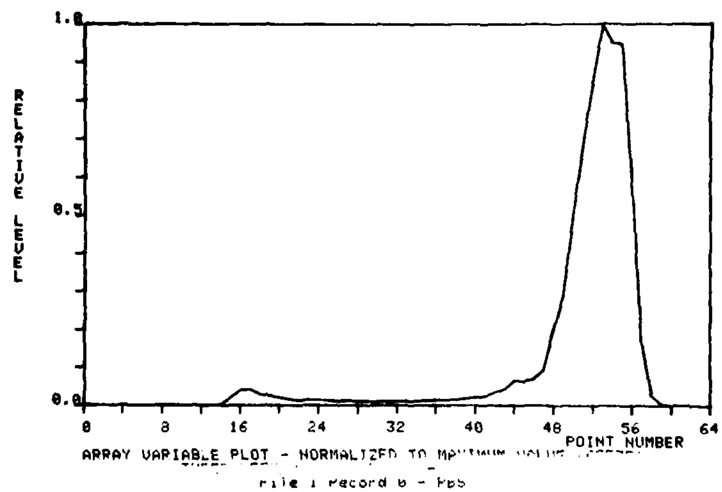


Figure C9. Typewritten text – pel brightness histogram (PBS).

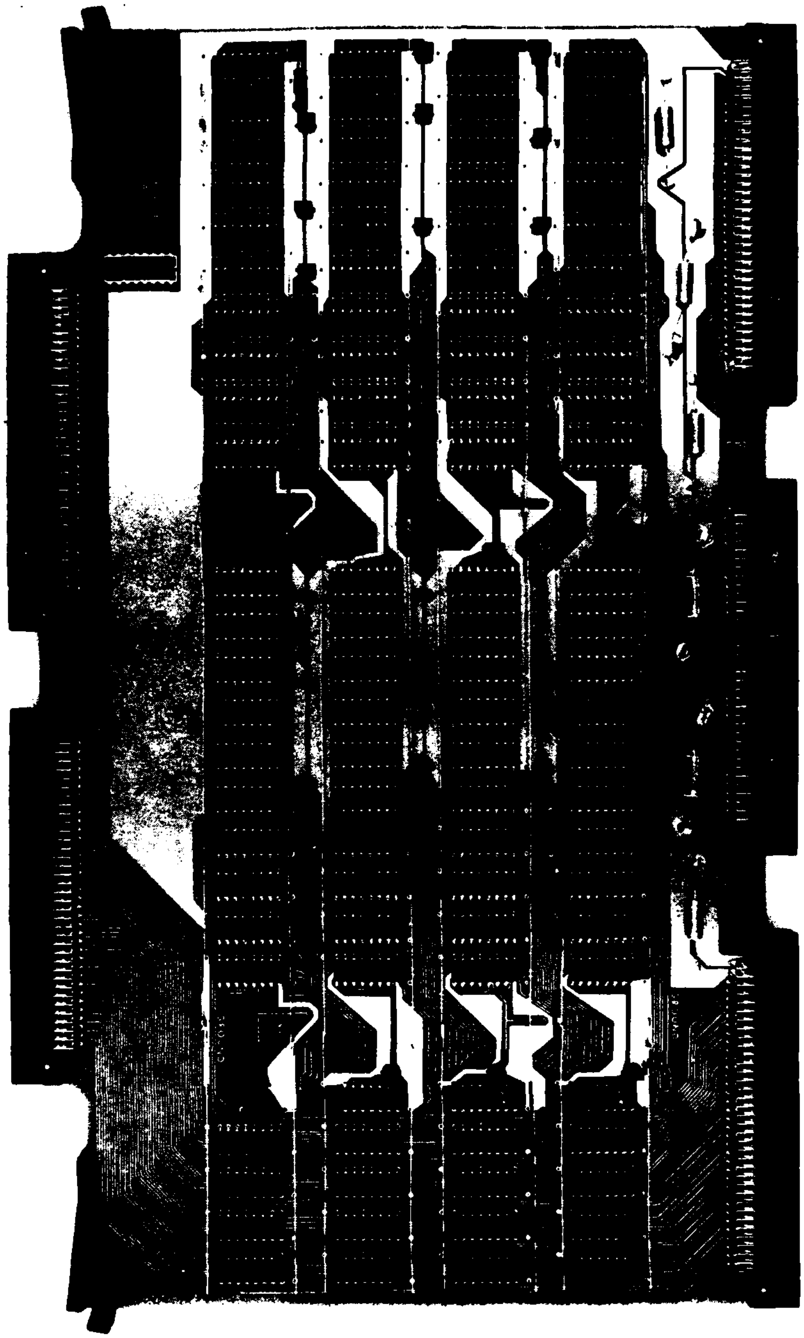


Figure C10. Circuit board photograph.

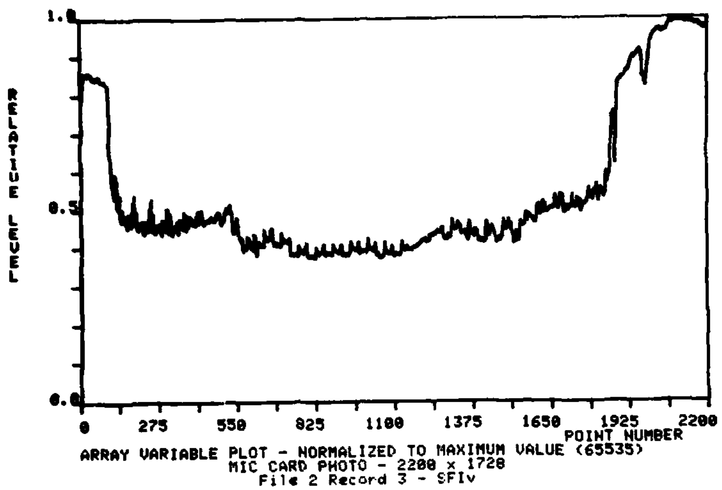


Figure C11. Circuit board card photograph – vertical brightness sum (SFI_v).

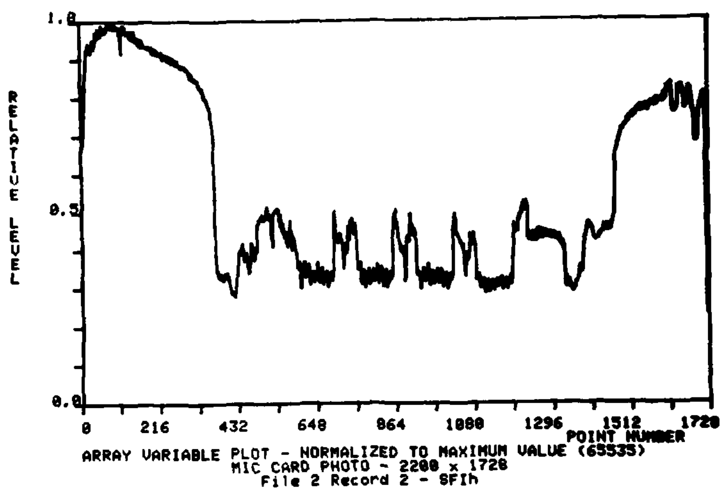


Figure C12. Circuit board card photograph – horizontal brightness sum (SFI_h).

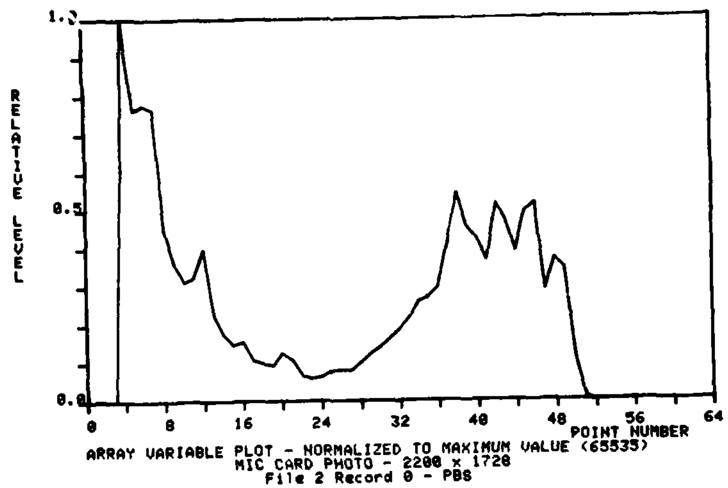


Figure C13. Circuit board photograph-pel brightness histogram (PBS).

Figure C14. IEEE facsimile test chart.

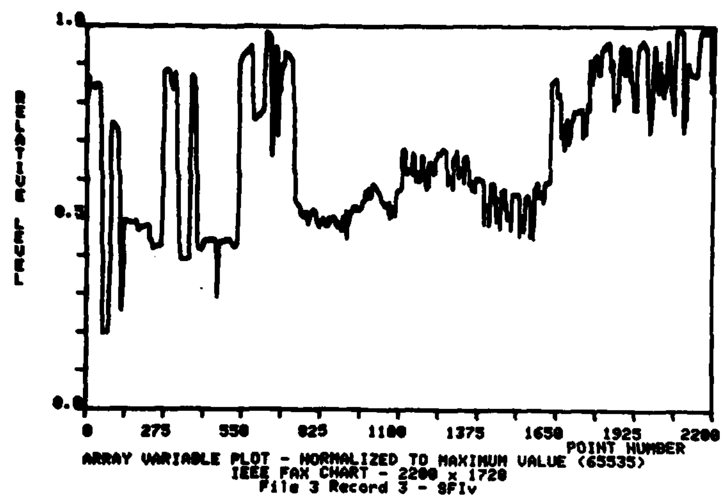


Figure C15. IEEE facsimile test chart – vertical brightness sum (SFI_v).

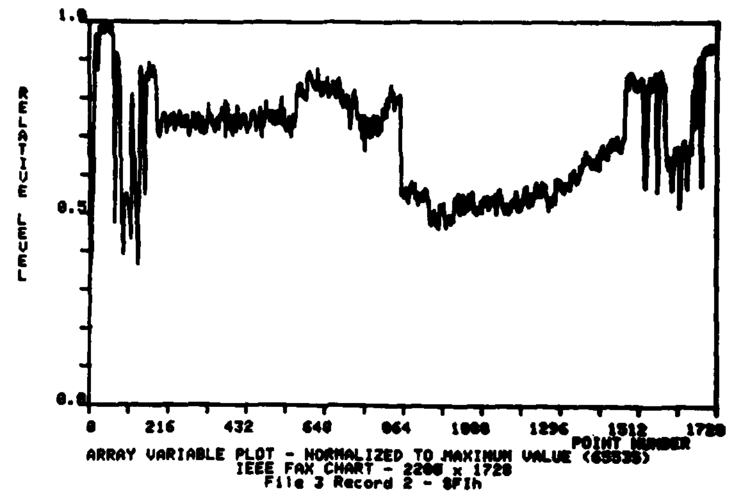


Figure C16. IEEE facsimile test chart – horizontal brightness sum (SFI_h).

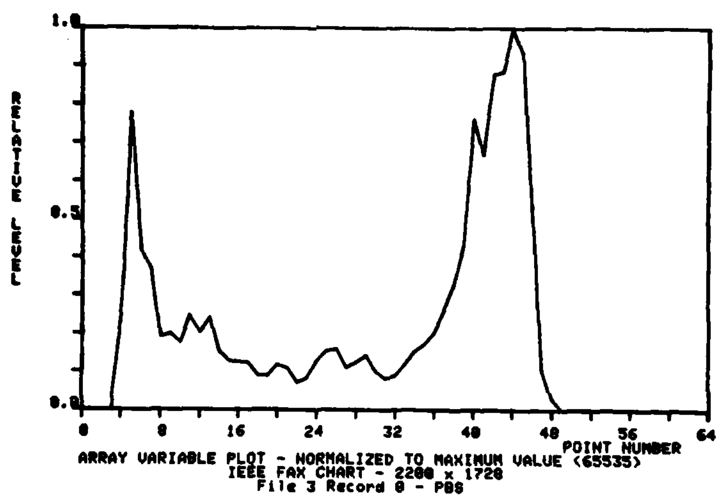


Figure C17. IEEE facsimile test chart – pel brightness histogram (PBS).

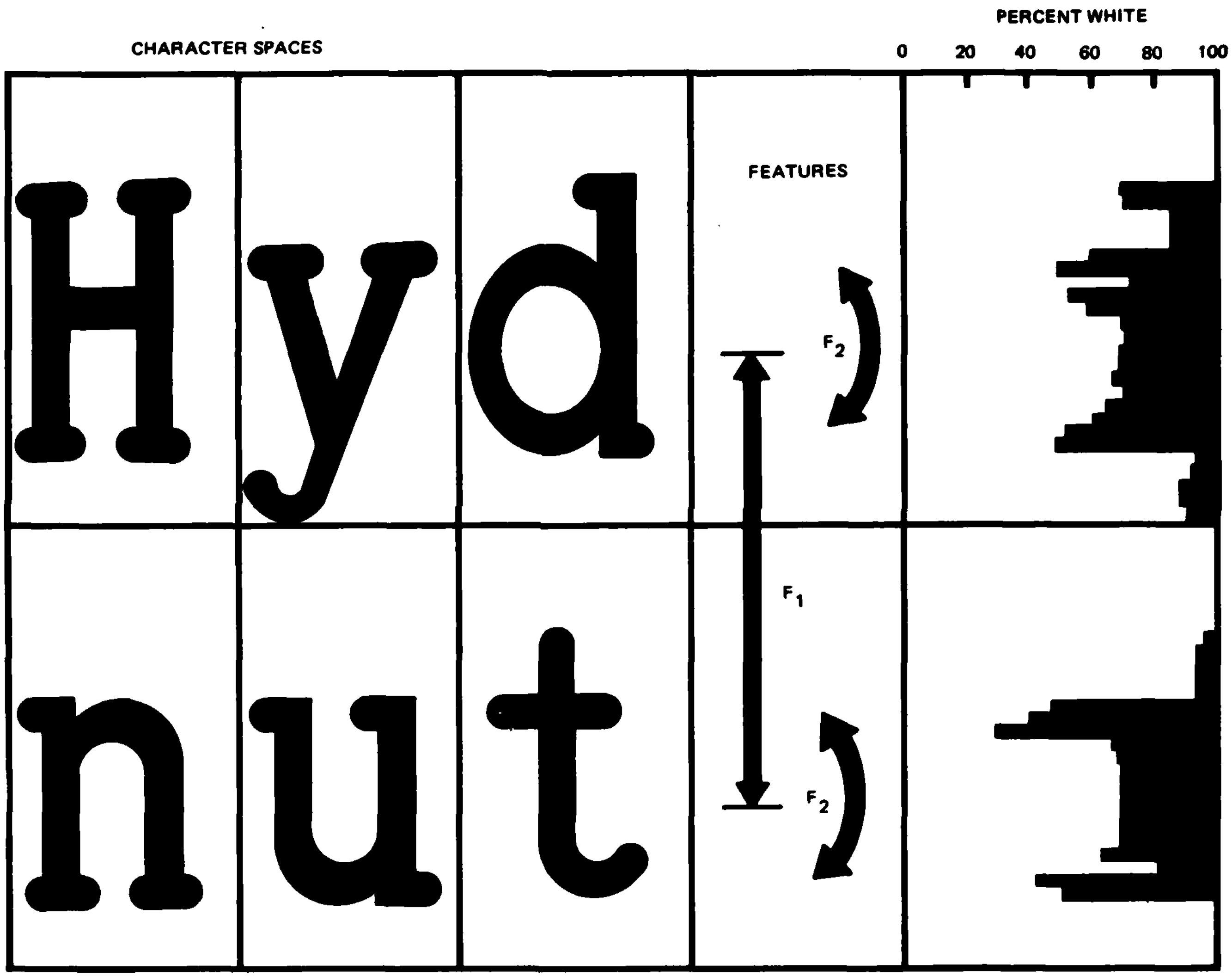


Figure C18. Detail of SFI_V statistic for typewritten text.

HORIZONTAL BRIGHTNESS SUM

The second pel brightness image statistic is the horizontal brightness sum, SFI_h. Like the vertical brightness sum, the SFI_h is the summation of pel brightness values – in this case those along each column of the scanned image. The presence of periodicities in the horizontal brightness sum statistic is heavily dependent on the degree of vertical alignment of characters between typewritten lines. If reasonable column alignment of characters is maintained by the output device, those periodicities will have a dominant spatial frequency component which can be detected and evaluated against spatial frequencies associated with standard character spacings. Thus, under this assumption, the utility of the SFI_h statistic will be much the same as that of the SFI_v statistic discussed previously for differentiating between photographic continuous-tone and typewritten images.

However, many present text generating output devices provide the capability for accommodating different character widths (eg, the character "i" is narrower than "W") and for right margin justification using noninteger character spacing. The result of variable spacing is to greatly reduce the effectiveness of the SFI_h statistic, since character spacing periodicities can be essentially averaged out in the vertical scan operation.

For this reason, care must be used in the interpretation of the SFI_h statistic. Basically, if the results indicate the presence of a valid spatial frequency component, then this information should contribute in a positive fashion towards a classification of typewritten material. However, lack of an appropriate spatial frequency component does not necessarily imply non-typewritten material.

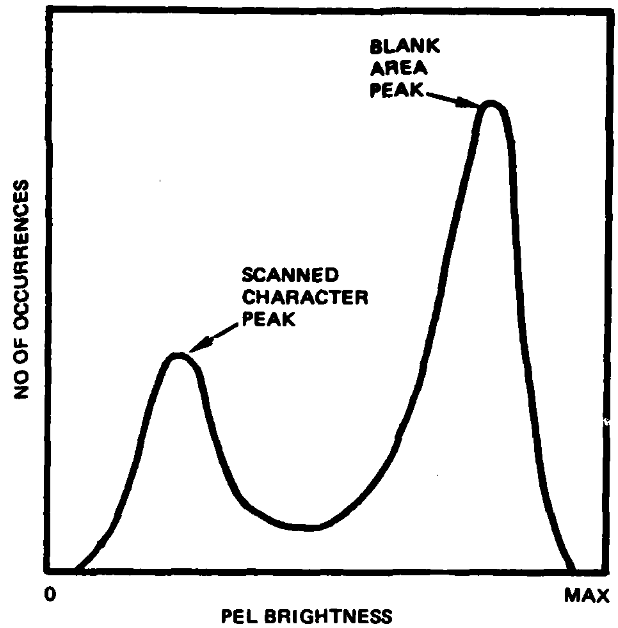
PEL BRIGHTNESS HISTOGRAM

The final principal image statistic is the frequency histogram of pel brightness values over the entire scanned image. The pel brightness statistic, PBS, for typewritten text is bimodal in nature. The largest concentration of brightness levels is centered about the average intensity level of blank areas of the scanned page. The second and smaller concentration of brightness values corresponds to the lower brightness levels of scanned typewritten characters. Between the two brightness level concentrations exists a fairly flat region of the histogram resulting from pels occurring at differing brightness values due to the essentially random pel positioning relative to individual character edges. Thus, in general, the PBS statistic for typewritten material will be bimodal, with a large number of high brightness level values and a discernible saddle point structure.

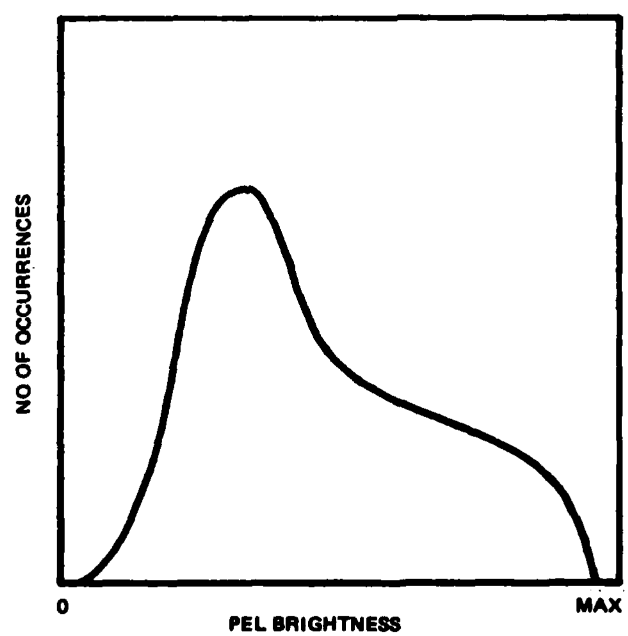
In contrast with the typewritten page, the PBS statistic for a continuous-tone photograph will be highly image dependent. This frequency histogram will normally be weighted towards the lower brightness values and will generally not be bimodal. For comparison purposes, examples of idealized pel brightness statistics for both typewritten and continuous-tone photographic images are shown in figure C19.

OTHER STATISTICAL IMAGE MEASURES

In addition to the three principal image statistics discussed above, a number of other measures have been proposed for image-type classification. Included in this category are frequency histograms of the brightness difference between adjacent pels, tests for local pel brightness maxima and minima values, and the use of pel brightness templates. To date,



A. TYPEWRITTEN TEXT IMAGE



B. CONTINUOUS-TONE IMAGE

Figure C19. Idealized pel brightness histograms.

none of these techniques for detecting image characteristics have been evaluated to determine their potential for automatic image-type classification applications.

AUTOMATIC CLASSIFICATION ALGORITHMS

VERTICAL SPATIAL FREQUENCY DETECTOR

The SFI_V statistic is well suited to FFT analysis methods for determining whether significant vertical spatial frequency components exist due to the spacing of typewritten lines. In these SFI_V evaluations, conventional windowing techniques are employed for the FFT operations to achieve near optimal side-lobe suppression (ref 2). The SFI_V statistic for a page consists of 2200 pel brightness sums (ie, 200 pels per inch x 11 inches). The most direct approach is to perform FFT processing on the center 2048-point subset of the SFI_V pel brightness sums. This represents a global approach and only permits a determination to be made as to whether or not the scanned image predominately contains lines of the correct spacing. No local information as to where the line structure(s) start or stop can be obtained from this method.

The presence of letterheads, paragraph spacings, signatures, etc, within standard letter formats produces some SFI_V brightness sums characteristic of nonuniform line spacings. Thus, the effectiveness of the FFT for isolating specific line spacing spatial frequencies from the original SFI_V data set will be somewhat reduced. As an alternative, a sliding partition approach has been used. This approach defines successive partition locations of length $N_V = 256$ along the SFI_V data set. This partition length corresponds to a vertical scanning interval of 1.28 inches, which, for single-space typing, contains approximately seven complete lines of text (actually 7.68 lines).

The standard FFT operation will result in the determination of the power (magnitude squared) for SFI_V spatial frequencies from dc to 100 cycles per inch. Within this range of spatial frequencies, single-space pages of typewritten text will produce spatial frequency components principally in the region centered about 6 cycles per inch. It should be noted that in potential hardware implementations of this scheme, significant FFT computational savings can be realized by computing the power for only those spatial frequencies known to be of importance for detecting line spacings.

For each partition location, the algorithm for detection of a given frequency component is based on computing the power within a pass band centered on the spatial frequency of interest. The total power within the pass band is compared against a threshold value. Exceeding the threshold implies the presence of a specific line spacing structure within that portion of the image covered by the partition. Sliding of the partition allows the power threshold comparison to be performed along the entire vertical extent of the scanned image.

The amount of displacement between adjacent partition locations has been nominally set at one-half the partition interval length. Overlapping the SFI_V data values in each FFT computation is done to compensate for the suppression of data values at the extremes of each partition interval due to windowing. For the 2200-point array of SFI_V values, a

2. FJ Harris, On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform, Proc of the IEEE, vol 66, no 1, January 1978

sliding partition with a 50% overlap results in 16 separate pass band power computations and threshold comparisons.

An ad hoc rule has been formulated for using the SFI_v statistic. The rule is that if either:

> The pass band power threshold is exceeded for at least two consecutive partition locations

or

> The pass band power threshold is exceeded for any four partition locations

then a line spacing periodicity typical of typewritten text has been detected in the scanned image.

HORIZONTAL SPATIAL FREQUENCY DETECTOR

Analysis of the SFI_h statistic also lends itself to FFT methods. In this case, however, the spatial frequencies of interest correspond to individual character spacing. The SFI_h statistic consists of 1728 columnwise brightness sums. The sliding partition approach is also used in the analysis of the SFI_h statistic. Here, the partition length has been set at N_h = 128 points and corresponds to a horizontal scanning interval of 0.64 inch, or approximately seven spaces of 12-pitch typewritten characters.

The approach for determining the presence of a horizontal spatial frequency component is essentially identical to that employed for the SFI_v statistic. The power at each partition location within a pass band centered on the specified character spacing spatial frequency – eg, 12 cycles per inch – is computed and compared against a threshold value. With the use of a 50% overlap, 26 separate band pass power computations and threshold comparisons result for the 1728 SFI_h statistic data values. Exceeding the threshold value indicates the presence of a vertical structure of proper typewritten character spacing for that partition location. The SFI_h statistic detection procedure is based on the following ad hoc rule. If:

> The pass band power threshold is exceeded for any partition location

then a periodicity representative of typewritten character spacing has been detected in the scanned image.

SADDLE POINT DETECTOR

Use of the PBS frequency histogram statistic for image-type classification requires a significantly different approach from that employed for analysis of the SFI_v and SFI_h statistics. The PBS statistic does not contain periodicity information but instead reflects the number of occurrences at each pel brightness value. As noted previously, the PBS statistic for typewritten text is characterized by two concentrations or peaks of pel brightness value occurrences with a minimum or saddle point in between. As an example, figure C20 shows the pel brightness histogram of a typewritten text test image. In this figure, the values for the blank area and typewritten character peaks are denoted as P_b and P_c, respectively. The number of pel brightness occurrences at each peak location is shown as $| P_b |$ and $| P_c |$. The location of the minimum number of pel brightness occurrences between the blank area and typewritten character peaks is identified as M_{bc}.

The PBS statistic algorithm is designed to detect the presence of this characteristic structure on the basis of pel brightness values and the number of occurrences for the two local maxima and the saddle point. The approach used is one of searching across the one-dimensional PBS array for the dynamic range of the pel brightness values and for the local maxima and saddle points. For typewritten text, the largest concentration of pel brightness values occurs for blank areas of the scanned page. Thus, the location of the maximum value of the PBS statistic corresponds to the location of the P_b peak. From this peak location, a sequential search is made in the direction of lower brightness values for the local minimum, M_{bc}, and the second local maximum, P_c. The initial step of the search is made large in order to minimize the likelihood of selecting a side lobe of the maximum value peak as the second local maximum. Local PBS value averaging can be used in conjunction with the search process to smooth out noise spikes or other transients in the data which could result in incorrect determinations of local maxima and minimum value locations.

The result of this analysis is the determination of the number of occurrences and the pel brightness values for the two local maxima and the local minimum and the dynamic range

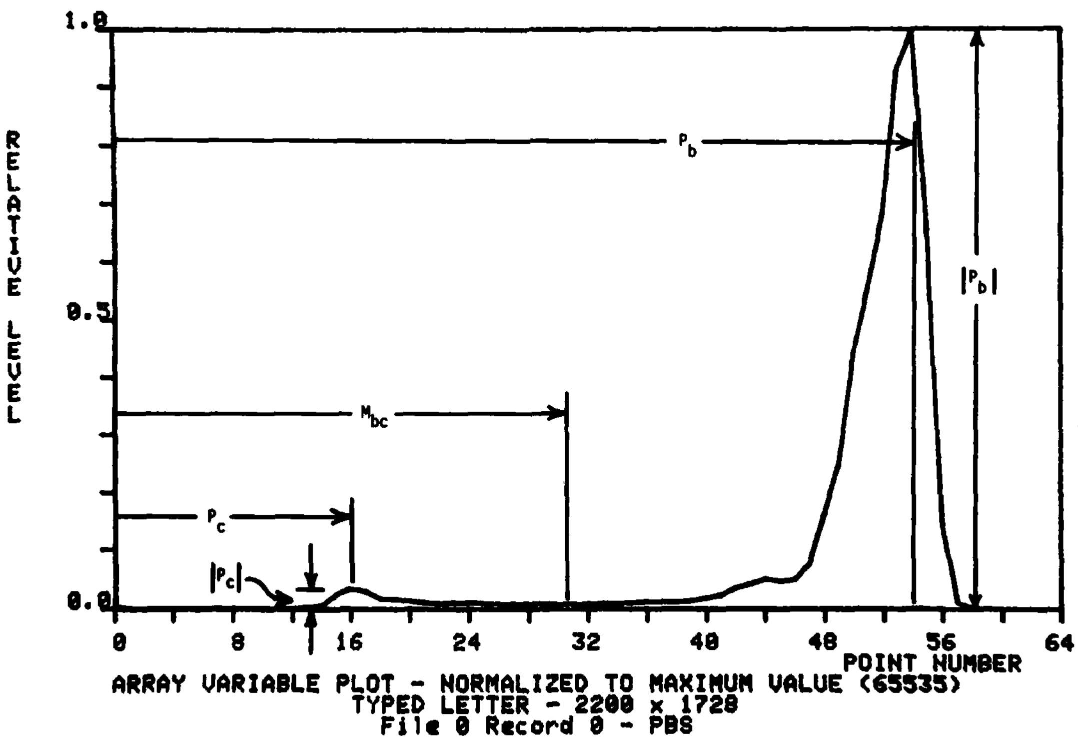


Figure C20. Typewritten text – analysis of pel brightness histogram (PBS).

of the pel brightness values. From this information, the following criteria for the pel brightness statistic have been formulated. If:

1. The blank area pel brightness peak, P_b, is within the highest one-third of the pel brightness dynamic range

2. The typewritten character pel brightness peak, P_c, is within the lowest one-third of the pel brightness dynamic range

3. The saddle point local pel brightness minimum, M_{bc}, is within the middle one-half of the pel brightness dynamic range

and

4. The number of pel brightness occurrences for the blank area peak $|P_b|$ exceeds the number of occurrences for the typewritten character peak $|P_c|$ by at least a factor of 10

then the scanned image is considered to be representative of typewritten text.

CLASSIFICATION STRATEGY

Classification of a scanned image is based on the following interpretation of the SFI_v, SFI_h, and PBS statistics. If the scanned image exhibits:

1. A vertical periodicity representative of typewritten text line spacing
2. A horizontal periodicity representative of typewritten text character spacing

and

3. A pel brightness histogram representative of typewritten text

then the scanned image is classified as being typewritten text and suitable for coding through binary thresholding. Failure to satisfy one or more of these conditions implies the requirement for 6-bit resolution coding of the image.

PRELIMINARY ANALYSIS RESULTS

A preliminary evaluation of the SFI_v, SFI_h, and PBS image statistics for classifying typewritten text and photographic images has been performed. The nonjustified and justified typewritten text images and the circuit board and IEEE facsimile test chart photographic images were used. For these four cases, the image statistics permitted the correct classification to be made for each test image. Image classification was based on the ad hoc rules for analysis of the image statistics and on the classification strategy defined in the previous sections.

The analysis performed on the typewritten text image without justification is considered first. In this analysis, sliding partition techniques were applied to both the SFI_v and SFI_h statistics. For convenience, figures C21 through C23 show numbered vertical and horizontal partition locations on the typewritten text image and on the corresponding SFI_v and SFI_h image statistics.

Examples of the FFT analysis of the SFI_v statistic at partition locations 1,4, and 6 are given as figures C24 through C26. These figures also illustrate the pass band interval of

10 April 1980
467A

Mr. W. T. Marable, Executive Director
Research & Development Laboratories
11711 Parklawn Avenue
Rockville, Maryland 20852

Gentlemen:

This is a sample of a letter we use as a "standard" for imaging experiments at NOSC, San Diego. It was made on a Wang Word Processor 30, and printed with a Wang Model 5581 Daisy Printer. The keystroke information is recorded on a 10 megabyte sealed disk in United States of America Standard Code for Information Interchange (USASCII) format. This is a standard seven-bit (plus parity) binary code for each keystroke which is widely used in industry. In USASCII form, this page as written can be exactly defined by 1777 characters (14216 bits) of data (excluding signature, logo, or header information). When scanned at 200-by-200 picture elements per inch with six bits per element for grey scale, the page is defined by 22,440,000 bits.

By recording this letter on the hard disk (and/or on the archive single diskette), it is possible to reproduce a quantity of duplicate originals, all nominally identical. Since the printer is a modified Xerox Diablo typewriter, it is also possible to change ribbons (a five-minute process) to yield copies of differing colors. It is of course possible to write on all textures, colors and weights of paper with or without letter head. It will also allow copies of this text to be analyzed both with and without signatures of various colors.

This ability to provide complete parameter selection and consistency control for analysis of thresholds, contrasts, color separation, compressibility coefficients, and character fonts will be of great benefit in quantifying the requirements of U. S. Postal Service scanner technology.

Frank Martin
NOSC Code 7323
Problem EE25

SFI_v PARTITION LOCATIONS

SFI_h PARTITION LOCATIONS

Figure C21. Typewritten text without justification — SFI_v and SFI_h partition locations.

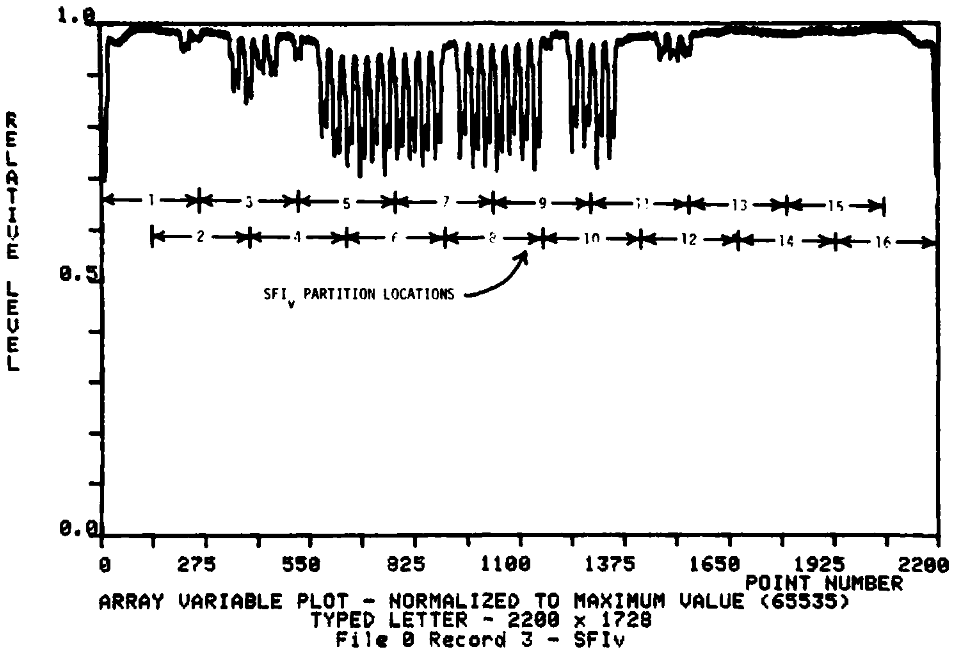


Figure C22. Typewritten text without justification – SFI$_v$ partition locations.

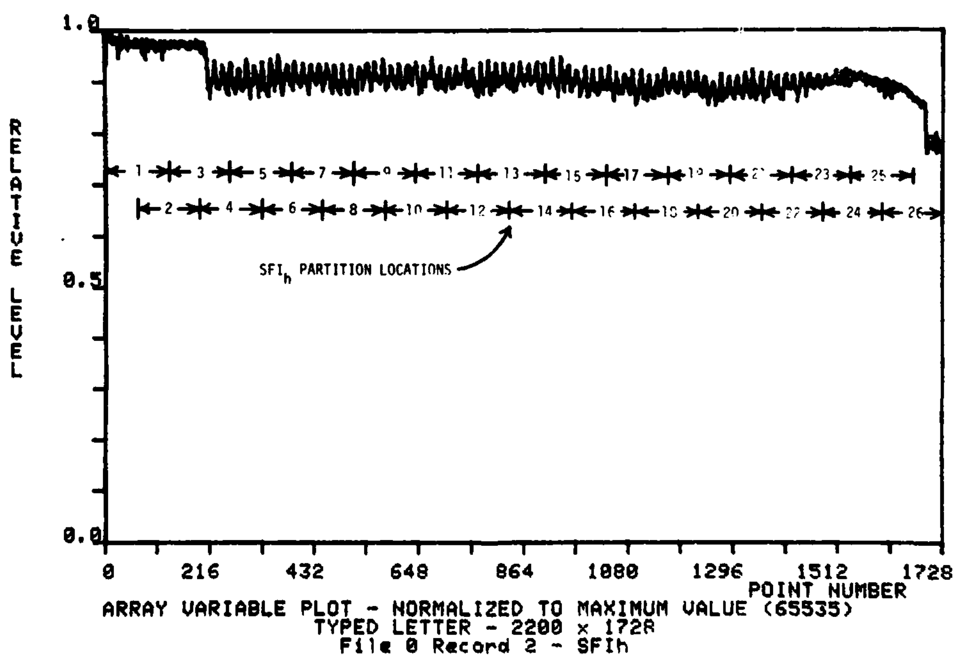


Figure C23. Typewritten text without justification – SFI$_h$ partition locations.

HORIZONTAL BRIGHTNESS SUM

The second pel brightness image statistic is the horizontal brightness sum, SFI_h. Like the vertical brightness sum, the SFI_h is the summation of pel brightness values – in this case those along each column of the scanned image. The presence of periodicities in the horizontal brightness sum statistic is heavily dependent on the degree of vertical alignment of characters between typewritten lines. If reasonable column alignment of characters is maintained by the output device, those periodicities will have a dominant spatial frequency component which can be detected and evaluated against spatial frequencies associated with standard character spacings. Thus, under this assumption, the utility of the SFI_h statistic will be much the same as that of the SFI_v statistic discussed previously for differentiating between photographic continuous-tone and typewritten images.

However, many present text generating output devices provide the capability for accommodating different character widths (eg, the character "i" is narrower than "W") and for right margin justification using noninteger character spacing. The result of variable spacing is to greatly reduce the effectiveness of the SFI_h statistic, since character spacing periodicities can be essentially averaged out in the vertical scan operation.

For this reason, care must be used in the interpretation of the SFI_h statistic. Basically, if the results indicate the presence of a valid spatial frequency component, then this information should contribute in a positive fashion towards a classification of typewritten material. However, lack of an appropriate spatial frequency component does not necessarily imply non-typewritten material.

PEL BRIGHTNESS HISTOGRAM

The final principal image statistic is the frequency histogram of pel brightness values over the entire scanned image. The pel brightness statistic, PBS, for typewritten text is bimodal in nature. The largest concentration of brightness levels is centered about the average intensity level of blank areas of the scanned page. The second and smaller concentration of brightness values corresponds to the lower brightness levels of scanned typewritten characters. Between the two brightness level concentrations exists a fairly flat region of the histogram resulting from pels occurring at differing brightness values due to the essentially random pel positioning relative to individual character edges. Thus, in general, the PBS statistic for typewritten material will be bimodal, with a large number of high brightness level values and a discernible saddle point structure.

In contrast with the typewritten page, the PBS statistic for a continuous-tone photograph will be highly image dependent. This frequency histogram will normally be weighted towards the lower brightness values and will generally not be bimodal. For comparison purposes, examples of idealized pel brightness statistics for both typewritten and continuous-tone photographic images are shown in figure C19.

OTHER STATISTICAL IMAGE MEASURES

In addition to the three principal image statistics discussed above, a number of other measures have been proposed for image-type classification. Included in this category are frequency histograms of the brightness difference between adjacent pels, tests for local pel brightness maxima and minima values, and the use of pel brightness templates. To date,

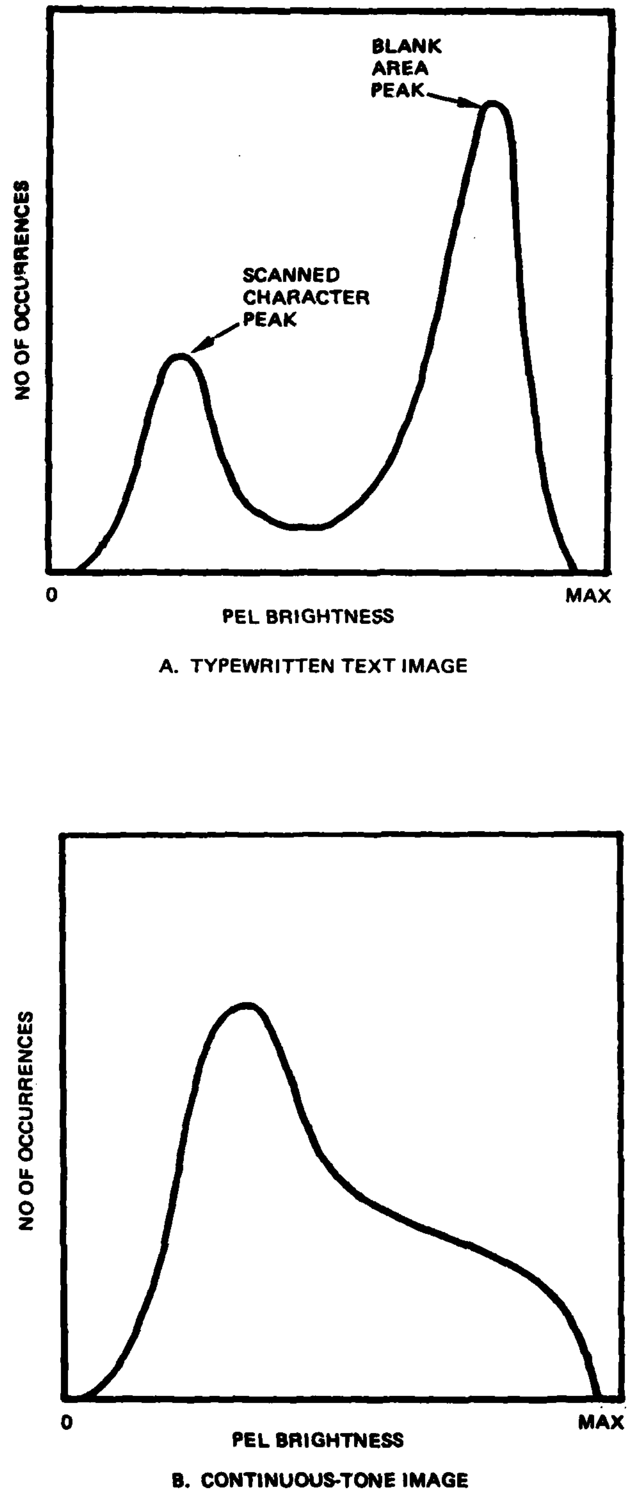


Figure C19. Idealized pel brightness histograms.

none of these techniques for detecting image characteristics have been evaluated to determine their potential for automatic image-type classification applications.

AUTOMATIC CLASSIFICATION ALGORITHMS

VERTICAL SPATIAL FREQUENCY DETECTOR

The SFI_V statistic is well suited to FFT analysis methods for determining whether significant vertical spatial frequency components exist due to the spacing of typewritten lines. In these SFI_V evaluations, conventional windowing techniques are employed for the FFT operations to achieve near optimal side-lobe suppression (ref 2). The SFI_V statistic for a page consists of 2200 pel brightness sums (ie, 200 pels per inch x 11 inches). The most direct approach is to perform FFT processing on the center 2048-point subset of the SFI_V pel brightness sums. This represents a global approach and only permits a determination to be made as to whether or not the scanned image predominately contains lines of the correct spacing. No local information as to where the line structure(s) start or stop can be obtained from this method.

The presence of letterheads, paragraph spacings, signatures, etc, within standard letter formats produces some SFI_V brightness sums characteristic of nonuniform line spacings. Thus, the effectiveness of the FFT for isolating specific line spacing spatial frequencies from the original SFI_V data set will be somewhat reduced. As an alternative, a sliding partition approach has been used. This approach defines successive partition locations of length $N_V = 256$ along the SFI_V data set. This partition length corresponds to a vertical scanning interval of 1.28 inches, which, for single-space typing, contains approximately seven complete lines of text (actually 7.68 lines).

The standard FFT operation will result in the determination of the power (magnitude squared) for SFI_V spatial frequencies from dc to 100 cycles per inch. Within this range of spatial frequencies, single-space pages of typewritten text will produce spatial frequency components principally in the region centered about 6 cycles per inch. It should be noted that in potential hardware implementations of this scheme, significant FFT computational savings can be realized by computing the power for only those spatial frequencies known to be of importance for detecting line spacings.

For each partition location, the algorithm for detection of a given frequency component is based on computing the power within a pass band centered on the spatial frequency of interest. The total power within the pass band is compared against a threshold value. Exceeding the threshold implies the presence of a specific line spacing structure within that portion of the image covered by the partition. Sliding of the partition allows the power threshold comparison to be performed along the entire vertical extent of the scanned image.

The amount of displacement between adjacent partition locations has been nominally set at one-half the partition interval length. Overlapping the SFI_V data values in each FFT computation is done to compensate for the suppression of data values at the extremes of each partition interval due to windowing. For the 2200-point array of SFI_V values, a

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2. FJ Harris, On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform, Proc of the IEEE, vol 66, no 1, January 1978

sliding partition with a 50% overlap results in 16 separate pass band power computations and threshold comparisons.

An ad hoc rule has been formulated for using the SFI_v statistic. The rule is that if either:

> The pass band power threshold is exceeded for at least two consecutive partition locations

or

> The pass band power threshold is exceeded for any four partition locations

then a line spacing periodicity typical of typewritten text has been detected in the scanned image.

HORIZONTAL SPATIAL FREQUENCY DETECTOR

Analysis of the SFI_h statistic also lends itself to FFT methods. In this case, however, the spatial frequencies of interest correspond to individual character spacing. The SFI_h statistic consists of 1728 columnwise brightness sums. The sliding partition approach is also used in the analysis of the SFI_h statistic. Here, the partition length has been set at N_h = 128 points and corresponds to a horizontal scanning interval of 0.64 inch, or approximately seven spaces of 12-pitch typewritten characters.

The approach for determining the presence of a horizontal spatial frequency component is essentially identical to that employed for the SFI_v statistic. The power at each partition location within a pass band centered on the specified character spacing spatial frequency – eg, 12 cycles per inch – is computed and compared against a threshold value. With the use of a 50% overlap, 26 separate band pass power computations and threshold comparisons result for the 1728 SFI_h statistic data values. Exceeding the threshold value indicates the presence of a vertical structure of proper typewritten character spacing for that partition location. The SFI_h statistic detection procedure is based on the following ad hoc rule. If:

> The pass band power threshold is exceeded for any partition location

then a periodicity representative of typewritten character spacing has been detected in the scanned image.

SADDLE POINT DETECTOR

Use of the PBS frequency histogram statistic for image-type classification requires a significantly different approach from that employed for analysis of the SFI_v and SFI_h statistics. The PBS statistic does not contain periodicity information but instead reflects the number of occurrences at each pel brightness value. As noted previously, the PBS statistic for typewritten text is characterized by two concentrations or peaks of pel brightness value occurrences with a minimum or saddle point in between. As an example, figure C20 shows the pel brightness histogram of a typewritten text test image. In this figure, the values for the blank area and typewritten character peaks are denoted as P_b and P_c, respectively. The number of pel brightness occurrences at each peak location is shown as $|P_b|$ and $|P_c|$. The location of the minimum number of pel brightness occurrences between the blank area and typewritten character peaks is identified as M_{bc}.

The PBS statistic algorithm is designed to detect the presence of this characteristic structure on the basis of pel brightness values and the number of occurrences for the two local maxima and the saddle point. The approach used is one of searching across the one-dimensional PBS array for the dynamic range of the pel brightness values and for the local maxima and saddle points. For typewritten text, the largest concentration of pel brightness values occurs for blank areas of the scanned page. Thus, the location of the maximum value of the PBS statistic corresponds to the location of the P_b peak. From this peak location, a sequential search is made in the direction of lower brightness values for the local minimum, M_{bc}, and the second local maximum, P_c. The initial step of the search is made large in order to minimize the likelihood of selecting a side lobe of the maximum value peak as the second local maximum. Local PBS value averaging can be used in conjunction with the search process to smooth out noise spikes or other transients in the data which could result in incorrect determinations of local maxima and minimum value locations.

The result of this analysis is the determination of the number of occurrences and the pel brightness values for the two local maxima and the local minimum and the dynamic range

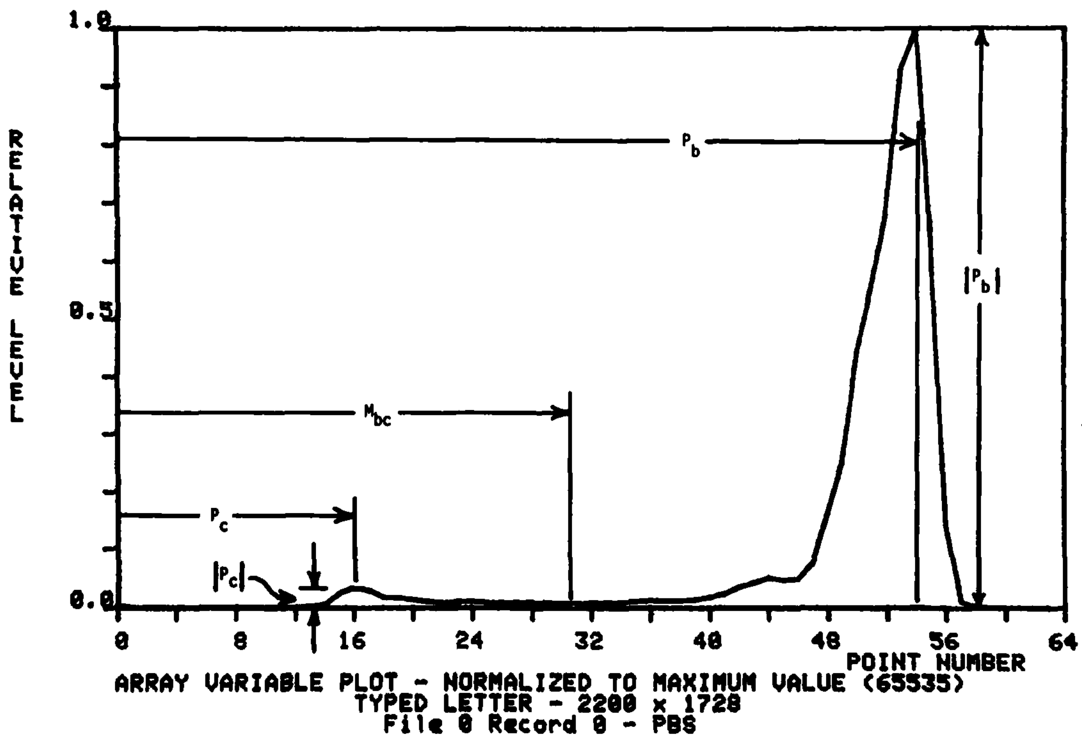

Figure C20. Typewritten text – analysis of pel brightness histogram (PBS).

of the pel brightness values. From this information, the following criteria for the pel brightness statistic have been formulated. If:

1. The blank area pel brightness peak, P_b, is within the highest one-third of the pel brightness dynamic range

2. The typewritten character pel brightness peak, P_c, is within the lowest one-third of the pel brightness dynamic range

3. The saddle point local pel brightness minimum, M_{bc}, is within the middle one-half of the pel brightness dynamic range

and

4. The number of pel brightness occurrences for the blank area peak $|P_b|$ exceeds the number of occurrences for the typewritten character peak $|P_c|$ by at least a factor of 10

then the scanned image is considered to be representative of typewritten text.

CLASSIFICATION STRATEGY

Classification of a scanned image is based on the following interpretation of the SFI_v, SFI_h, and PBS statistics. If the scanned image exhibits:

1. A vertical periodicity representative of typewritten text line spacing
2. A horizontal periodicity representative of typewritten text character spacing

and

3. A pel brightness histogram representative of typewritten text

then the scanned image is classified as being typewritten text and suitable for coding through binary thresholding. Failure to satisfy one or more of these conditions implies the requirement for 6-bit resolution coding of the image.

PRELIMINARY ANALYSIS RESULTS

A preliminary evaluation of the SFI_v, SFI_h, and PBS image statistics for classifying typewritten text and photographic images has been performed. The nonjustified and justified typewritten text images and the circuit board and IEEE facsimile test chart photographic images were used. For these four cases, the image statistics permitted the correct classification to be made for each test image. Image classification was based on the ad hoc rules for analysis of the image statistics and on the classification strategy defined in the previous sections.

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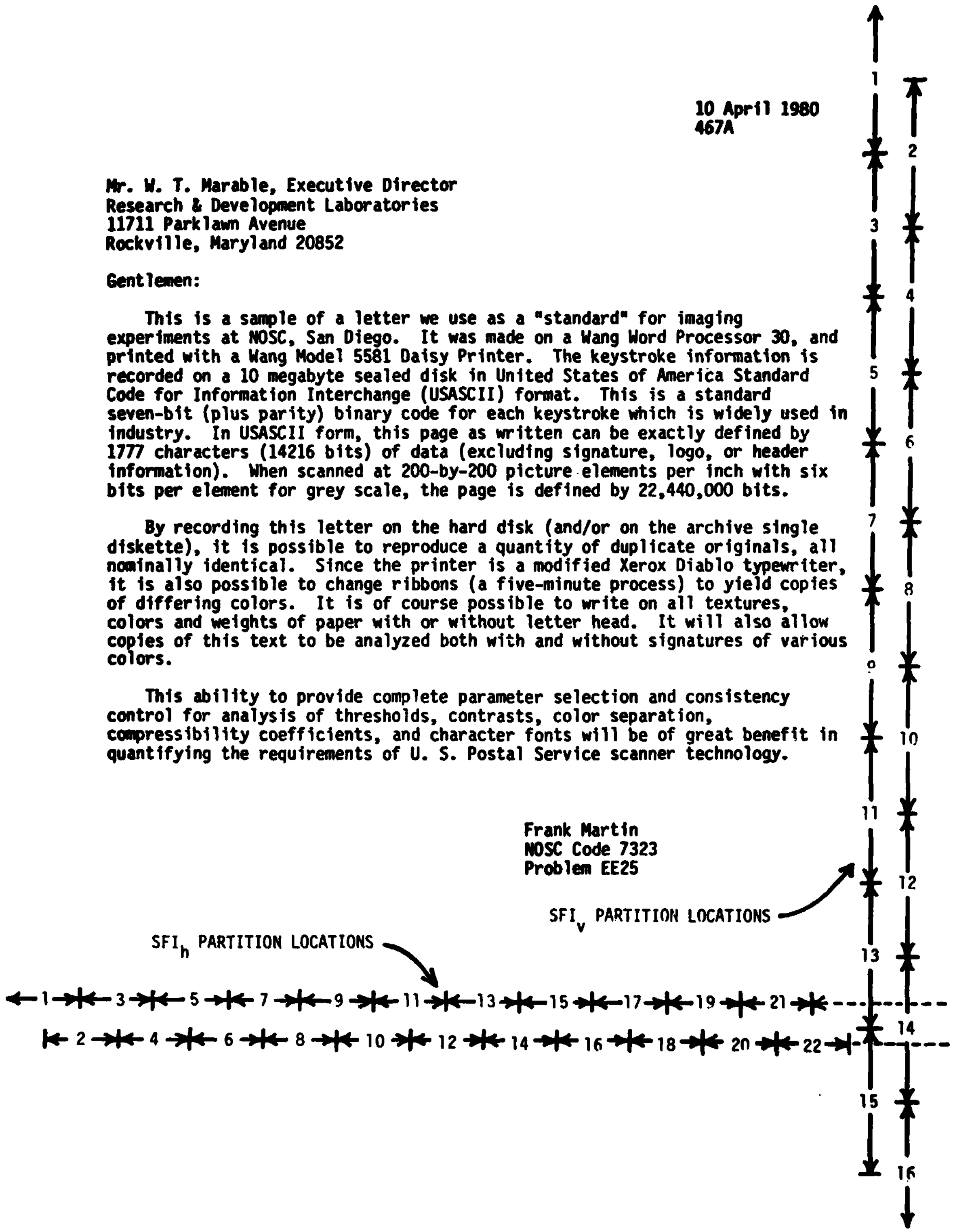

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Problem EE25

Figure C21. Typewritten text without justification – SFI_v and SFI_h partition locations.

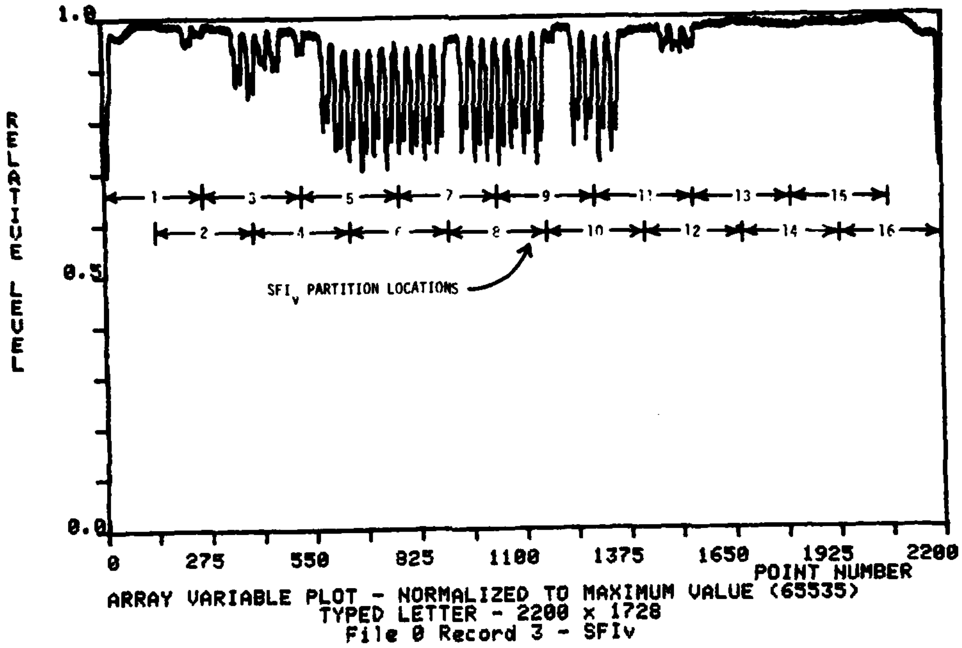

Figure C22. Typewritten text without justification – SFI$_v$ partition locations.

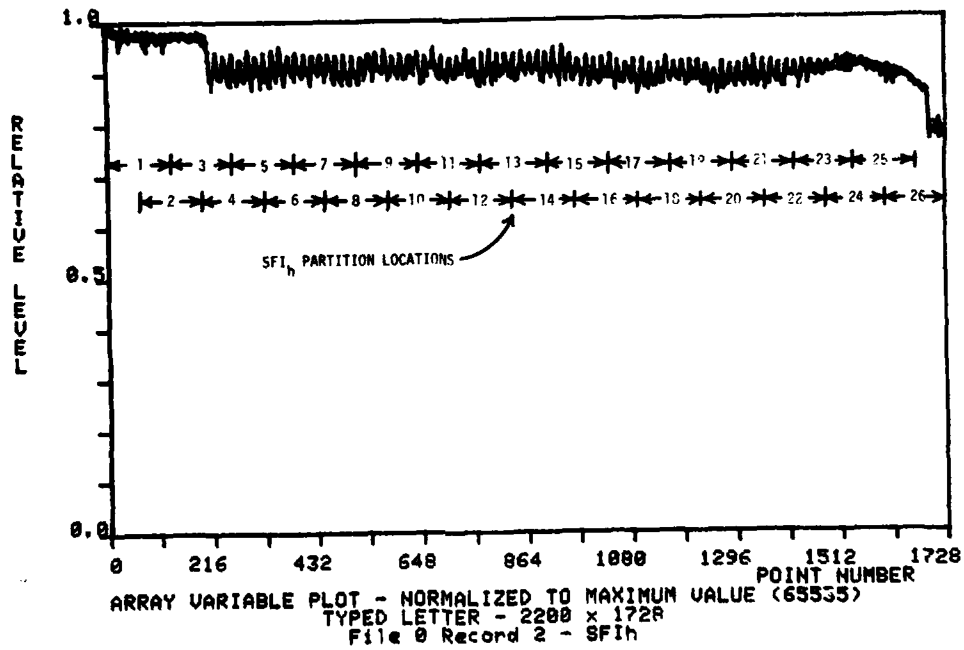

Figure C23. Typewritten text without justification – *SFI$_h$* partition locations.

SFI-V POWER VS
SPATIAL FREQUENCY

TYPEWRITTEN PAGE – 12 PITCH, SINGLE SPACE, WITHOUT JUSTIFICATION
PARTITION SIZE: 256
PARTITION LOCATION: 1
SAMPLES: 1 THROUGH 256

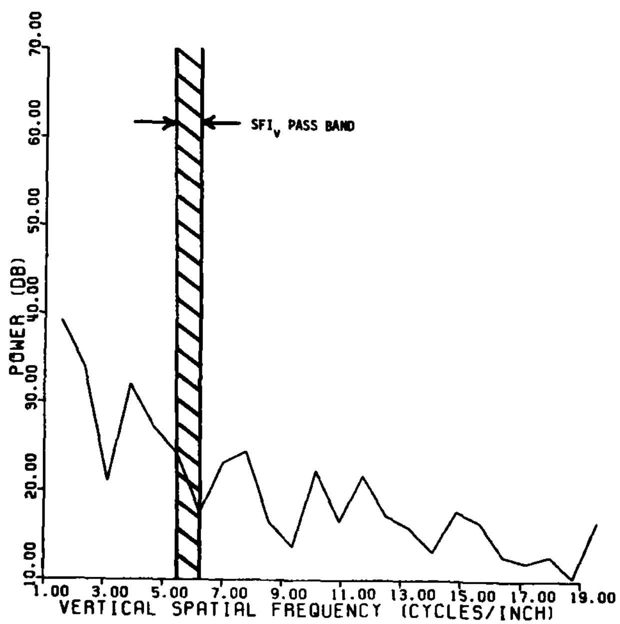

Figure C24. Typewritten text without justification – SFI_V power spectra at partition location 1.

SFI-V POWER VS
SPATIAL FREQUENCY

TYPEWRITTEN PAGE – 12 PITCH, SINGLE SPACE, WITHOUT JUSTIFICATION
PARTITION SIZE: 256
PARTITION LOCATION: 4
SAMPLES: 385 THROUGH 640

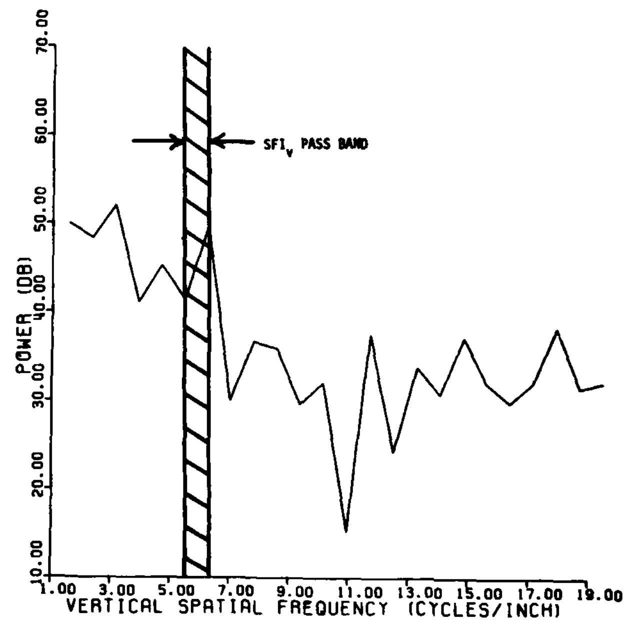

Figure C25. Typewritten text without justification – SFI_V power spectra at partition location 4.

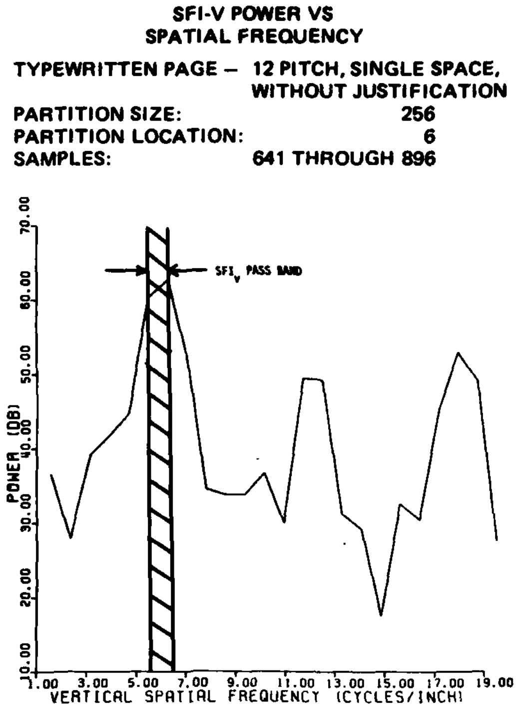

Figure C26. Typewritten text without justification – SFI_v power spectra at partition location 6.

interest for single-line spacing periodicities. Figure C24 represents the initial partition location at the top of the typewritten page of text. This partition location defines a region of the image which is blank except for a date and identification number at the extreme right. Consequently, no significant pass band power occurs for this partition location. Partition location 4 was used in the example of figure C25. Here, the partition interval covers some of the header material and a portion of the first paragraph. As expected, the pass band power for this partition location is considerably larger because of the presence of a partial line spacing structure. The third partition considered is at location 6. This corresponds to a partition interval which includes the maximum number of single-space typewritten lines. Figure C26 illustrates that the pass band power in this case is extremely high. These figures serve to illustrate the ability of the sliding partition method to detect local line spacing periodicities within a typewritten image.

In a similar fashion, the SFI_h statistic has also been analyzed. The results of FFT processing for partition location 10 are shown in figure C27. In this example, the pass band of interest corresponds to character spacing periodicities. Since vertical character alignment has been maintained in this test image, the properties of the SFI_h statistic are essentially unchanged for all partition locations which encompass regions of typewritten text.

Summary plots for the SFI_v and SFI_h statistics are shown in figures C28 and C29. These plots illustrate pass band power as a function of partition location. Examination of these figures shows a strong correspondence between regions of significant pass band power and areas of typewritten text in the input image. These plots form the basis for determining

SFI-H POWER VS
SPATIAL FREQUENCY

TYPEWRITTEN PAGE — 12 PITCH, SINGLE SPACE, WITHOUT JUSTIFICATION
PARTITION SIZE: 128
PARTITION LOCATION: 10
SAMPLES: 1153 THROUGH 1280

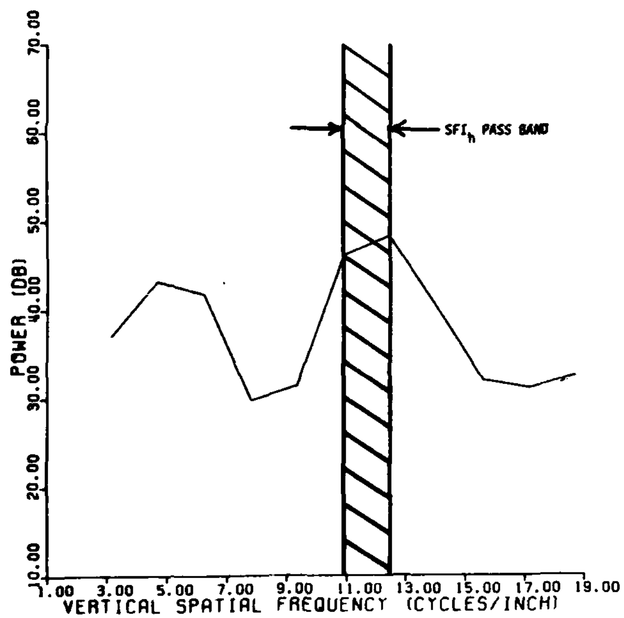

Figure C27. Typewritten text without justification — SFI$_h$ power spectra at partition location 10.

SFI-V PASS BAND POWER
VS PARTITION LOCATION

TYPEWRITTEN PAGE — 12 PITCH, SINGLE SPACE, WITHOUT JUSTIFICATION
PASS BAND: 5.47 THROUGH 6.25 CYCLES/INCH

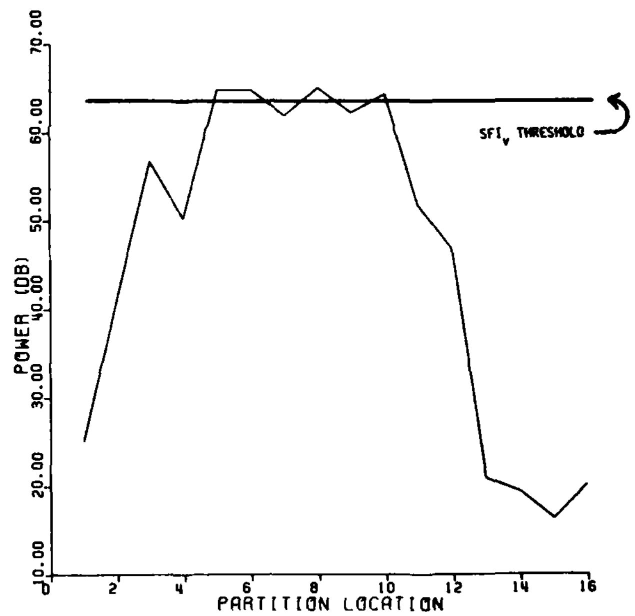

Figure C28. Typewritten text without justification — SFI$_v$ pass band power along vertical image extent.

SFI-H PASS BAND POWER
VS PARTITION LOCATION

TYPEWRITTEN PAGE – 12 PITCH, SINGLE SPACE, WITHOUT JUSTIFICATION

PASS BAND: 10.94 THROUGH 12.50 CYCLES/INCH

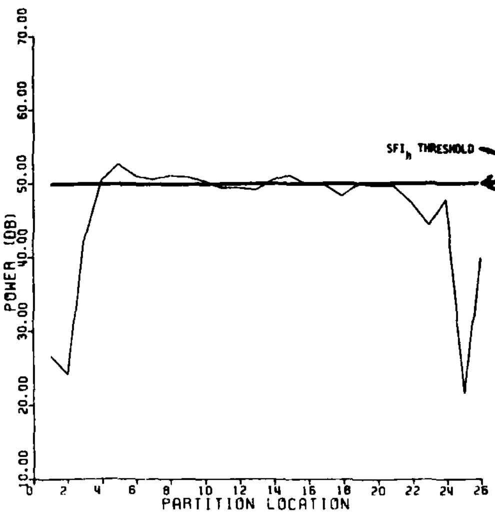

Figure C29. Typewritten text without justification – SFI_h pass band power along horizontal image extent.

whether line spacing and character spacing periodicities are present within a scanned input image. In this preliminary evaluation, thresholds of 2.0 x 10^6 and 1.0 x 10^5 were applied to the SFI_v and SFI_h pass band power. These threshold values are based on the computed SFI_v and SFI_h pass band power for the four test images and have been set near the maximum typewritten text image levels to provide optimum discrimination from the nontextual circuit board and IEE facsimile test chart images. The SFI_v and SFI_h pass band power threshold values used are also included in figures C28 and C29.

Selection of the SFI_v and SFI_h pass band power thresholds is crucial to the successful operation of the proposed EMSS image classification system. Since many image-to-image variations are expected, fixed thresholding schemes such as the one employed in this preliminary evaluation are generally not desirable. A threshold comparison method which may be appropriate is adaptive thresholding. Adaptive thresholding is commonly used in radar and other signal processing applications where input signal variations are expected to occur. In an adaptive thresholding system for image-type classification, the average power in adjacent pass band intervals would be compared with the power in the pass band of interest. Detection in this case would be based on the ratio of the power in the pass band of interest to the local average power. This approach, while still simple, would tend to minimize effects of variations between scanned input images.

The analysis of the second typewritten text image produces nearly identical results for the SFI_v statistic. However, the typewritten text for this image is right justified. This causes the SFI_h statistic to produce the strongest character spacing periodicities at the left and right margins of the text, with significant reductions in periodicity strength between the margins. This situation is illustrated in the summary plot of the SFI_h statistic given in figure C30. This plot shows that the maximum character spacing power occurs at the partition locations corresponding to the text margins, with decreasing levels of power between the margins. Thus, exceeding the SFI_h pass band power threshold at only these extreme partition locations is a valid indication of character spacing periodicity for this class of image.

Summary plots of the SFI_v and SFI_h statistics for the circuit board and IEEE facsimile test chart images are shown as figures C31 through C34. Neither of these images satisfies the SFI_v statistic analysis rules. In the case of the circuit board image, the SFI_v pass band power threshold is never exceeded, as shown in figure C31. The IEEE facsimile test chart image, however, does exceed the SFI_v pass band power threshold at partition location 2. Since this occurs only once within the image, the SFI_v statistic analysis rule is also not satisfied for this image. Thus, on the basis of the four test images, the SFI_v statistic appears to be useful for detecting line spacing periodicities.

By comparison, the SFI_h statistic was not successful in distinguishing between the typewritten and photographic test images investigated. In particular, the SFI_h pass band power threshold was exceeded on several occasions, as illustrated in figures C32 and C34. This fact, coupled with the less stringent conditions given for satisfying the SFI_h analysis rule, permitted both non-typewritten text images to incorrectly satisfy the conditions for the presence of character spacing periodicities.

The final statistic considered is the pel brightness histogram. The analysis of this image statistic involves searching the PBS data for the pel brightness occurrence peak corresponding to scanned blank areas, P_b, the secondary pel brightness occurrence peak for scanned typewritten characters, P_c, and the minimum brightness occurrence value between the peaks, M_{bc}. An additional measure extracted from the pel brightness statistic is the ratio of the number of occurrences at the blank area and typewritten character brightness peaks, $|P_b| / |P_c|$.

The PBS analysis results for the four test images are given in table C2. By applying the set of ad hoc rules defined previously, it can be seen that the histograms of the typewritten text images satisfy all the conditions for a textual image histogram. However, the histogram of the circuit board image does not satisfy these conditions, since no secondary maximum exists at a lower pel brightness value than that of the principal maximum. The IEEE facsimile test chart image histogram also fails the set of conditions for a textual image, since the $|P_b| / |P_c|$ ratio is less than 10.

CONCLUSIONS

Several conclusions and recommendations have been based on this preliminary evaluation of automatic image-type classification techniques. A major conclusion is that analysis of the SFI_v statistic for detecting line spacing periodicities and the pel brightness statistic for identifying typewritten text histogram properties can be successfully automated. In addition, classification of scanned input images based on these two statistical measures appears promising. A closely related conclusion is that the SFI_h statistic appears to be relatively ineffective for identifying instances in which strong character spacing periodicities exist.

The preliminary evaluation performed here involved only the analysis of single-space, 12-pitch typewritten text images. It should be noted that these techniques can be readily extended to include all expected combinations of space-and-a-half and double spacing with 10- and 12-pitch character spacing.

SFI-H PASS BAND POWER
VS PARTITION LOCATION

TYPEWRITTEN PAGE – 12 PITCH, SINGLE SPACE, WITH JUSTIFICATION

PASS BAND: 10.94 THROUGH 12.50 CYCLES/INCH

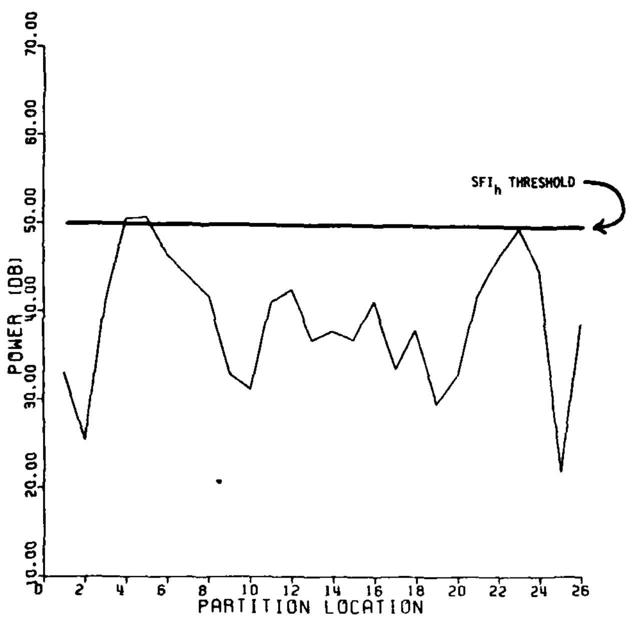

Figure C30. Typewritten text with justification – SFI_h pass band power along horizontal image extent.

SFI-V PASS BAND POWER
VS PARTITION LOCATION

CIRCUIT BOARD CARD PHOTOGRAPH

PASS BAND: 5.47 THROUGH 6.25 CYCLES/INCH

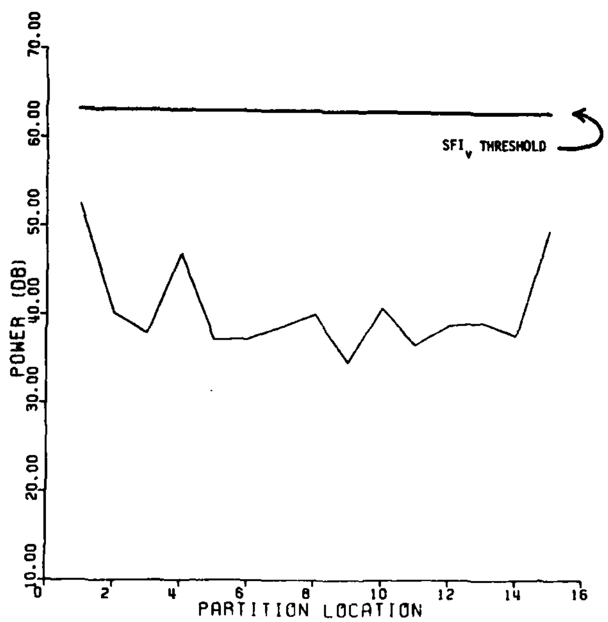

Figure C31. Circuit board photograph – SFI_v pass band power along vertical image extent.

SFI-H PASS BAND POWER
VS PARTITION LOCATION

CIRCUIT BOARD CARD PHOTOGRAPH

PASS BAND: 10.94 THROUGH 12.50 CYCLES/INCH

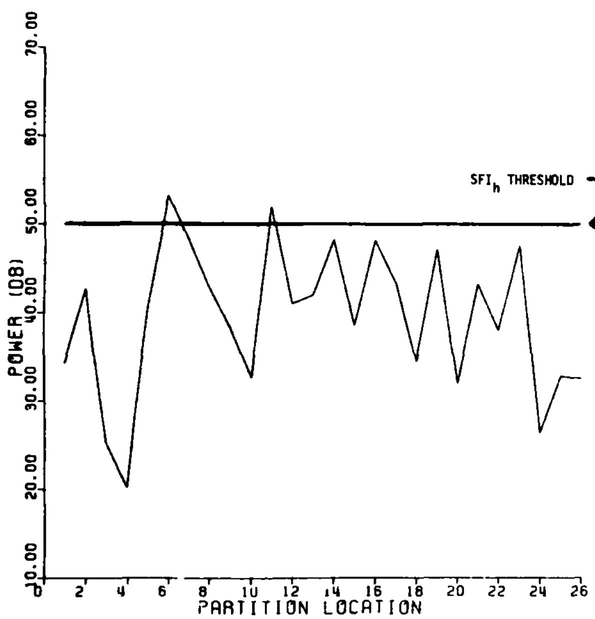

Figure C32. Circuit board photograph – SFI$_h$ pass band power along horizontal image extent.

SFI-V PASS BAND POWER
VS PARTITION LOCATION

IEEE FACSIMILE TEST CHART

PASS BAND: 5.47 THROUGH 6.25 CYCLES/INCH

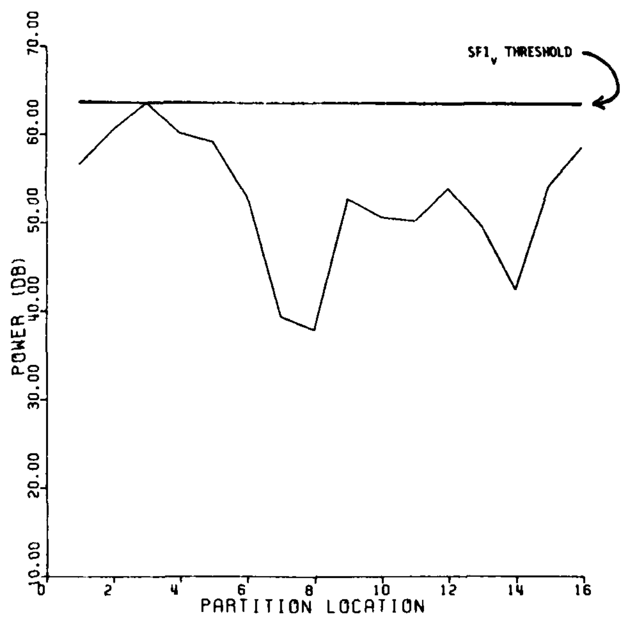

Figure C33. IEEE facsimile test chart – SFI$_v$ pass band power along vertical image extent.

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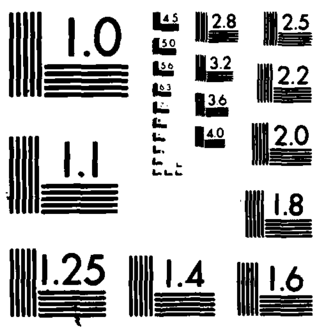
FILMED

DTIC



MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

SFI-H PASS BAND POWER
VS PARTITION LOCATION
IEEE FACSIMILE TEST CHART
PASS BAND: 10.94 THROUGH 12.50 CYCLES/INCH

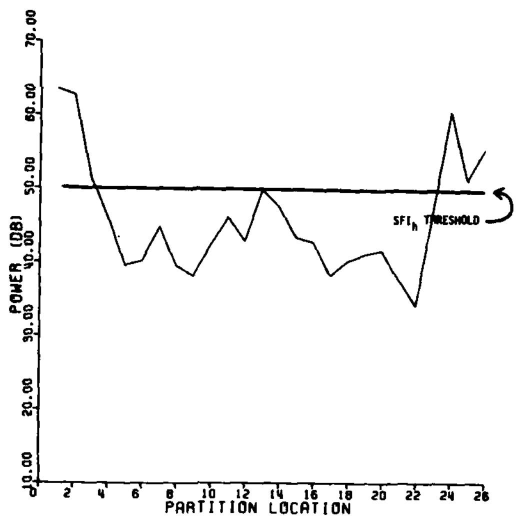


Figure C34. IEEE facsimile test chart – SFI_h pass band power along horizontal image extent.

Further investigations into automatic image-type classification techniques are recommended. Specifically, it is recommended that the techniques developed be applied to the set of test images collected during the FY78 NOSC/USPS program effort. Since this data set contains a broad assortment of typewritten text, printed form, and photographic images, the analysis of these images would provide a useful measure of performance for the automatic image type classification techniques developed here. In particular, it is expected that valuable experience would be gained regarding the choice of parameter settings and thresholding values for performing the image classification operation. Also, new image statistics need to be developed and evaluated to determine their potential value for image classification.

Typewritten text – single space, 12 pitch, without justification

P_b intensity	54
P_c intensity	16
M_{bc} intensity	31
$\lvert P_b \rvert / \lvert P_c \rvert$	29.07

Typewritten text - single space, 12 pitch, with justification

P_b intensity	53
P_c intensity	16
M_{bc} intensity	31
$\lvert P_b \rvert / \lvert P_c \rvert$	25.15

Circuit board photograph

P_b intensity	4
P_c intensity	N/A
M_{bc} intensity	N/A
$\lvert P_b \rvert / \lvert P_c \rvert$	N/A

IEEE facsimile test chart

P_b intensity	44
P_c intensity	5
M_{bc} intensity	22
$\lvert P_b \rvert / \lvert P_c \rvert$	1.29

Table C2. Pel brightness histogram statistic summary for test images.

APPENDIX D:

IMAGE CAPTURE AND ANALYSIS SYSTEM UPGRADE AND OPERATION

by

Lee A Wise

Robert W Basinger

Code 7323

July 1980

CONTENTS

ILLUSTRATIONS

TABLES

APPENDIX D GLOSSARY

A/D	analog to digital
AWG	American wire gage
CRT	cathode ray tube
DBSC	data bus switch card
DCC	display control card
DMA	direct memory access
DOS	Disk operating system
EMS	Electronic Message Service
FSM	Frame-store memory
GPIB	General purpose interface bus
IC	integrated circuit
ICAS	Image Capture and Analysis System
LDTB	Large drum test bed
MCU	Memory control unit
MDB	multiplexed data bus
MIC	memory interface cards
MICC-1, MICC-2	memory interface control cards
MIU	Memory Interface Unit
PC	Personality chassis; printed circuit
RQB	Conrac model RQB monitor
TSB	tristate buffer
TTL	transistor-transistor logic

INTRODUCTION

The initial goals of NOSC's participation in the USPS Electronic Message Service (EMS) program were:

1. Provide technical consultation, equipment, and support services towards the development of the EMS system definition

2. Contribute to the selection of imaging devices and techniques and nondestructive compression techniques for storage and transmission

3. Act as consultants in the preparation of technical requirements and evaluation of equipment produced to meet them

Because the EMS system definition is well supported by others and contracts have been awarded for hardware development models, the emphasis at NOSC has been placed primarily on the test and evaluation of imaging devices and techniques as well as processing and compression techniques.

The result of this shifting emphasis has been a gradual evolution of the USPS/NOSC Image Capture and Analysis System (ICAS). The subject of this report, then, is the changes which have taken place in ICAS since the last ICAS report (ref 1). For information on the portion of ICAS which has remained unaltered, the reader is referred to that report. This report includes comparisons between FY77 and FY80 and the advantages of the FY80 configuration.

BACKGROUND

Initially, the ICAS was intended to be a testbed for imaging devices. Because the first tests were successful, as interests in areas of imaging other than devices have evolved, so has the ICAS. The first stage in ICAS development consisted of a small drum test bed scanner, a memory control unit (MCU) for the control of image capture and display, a one-eighth-page frame-store memory (FSM), and a video monitor. The minimal software which was produced was entered via front-panel switches.

FY77 CONFIGURATION

By FY77 ICAS had been expanded substantially. Interest in areas of imagery such as illumination correction, enhancement, and compression had necessitated the addition of considerable hardware and software to support the large volume of data being handled. Figure D1 shows the FY77 configuration.

The ICAS had become a primitive multi-processing system using a Tektronix 4051 graphic system as the ICAS system controller and the MCU as the main processor and peripheral handler. The decision had been made to increase the size of the FSM to hold a full 8 1/2-by-11 inch page. This required the design and implementation of a memory interface unit (MIU) to handle the different addressing schemes of software usage, the display function, and the direct memory access (DMA) capture which was necessary to

1. Third Annual Report - Advanced Mail Systems Scanner Technology, NOSC TR 270, October 1977

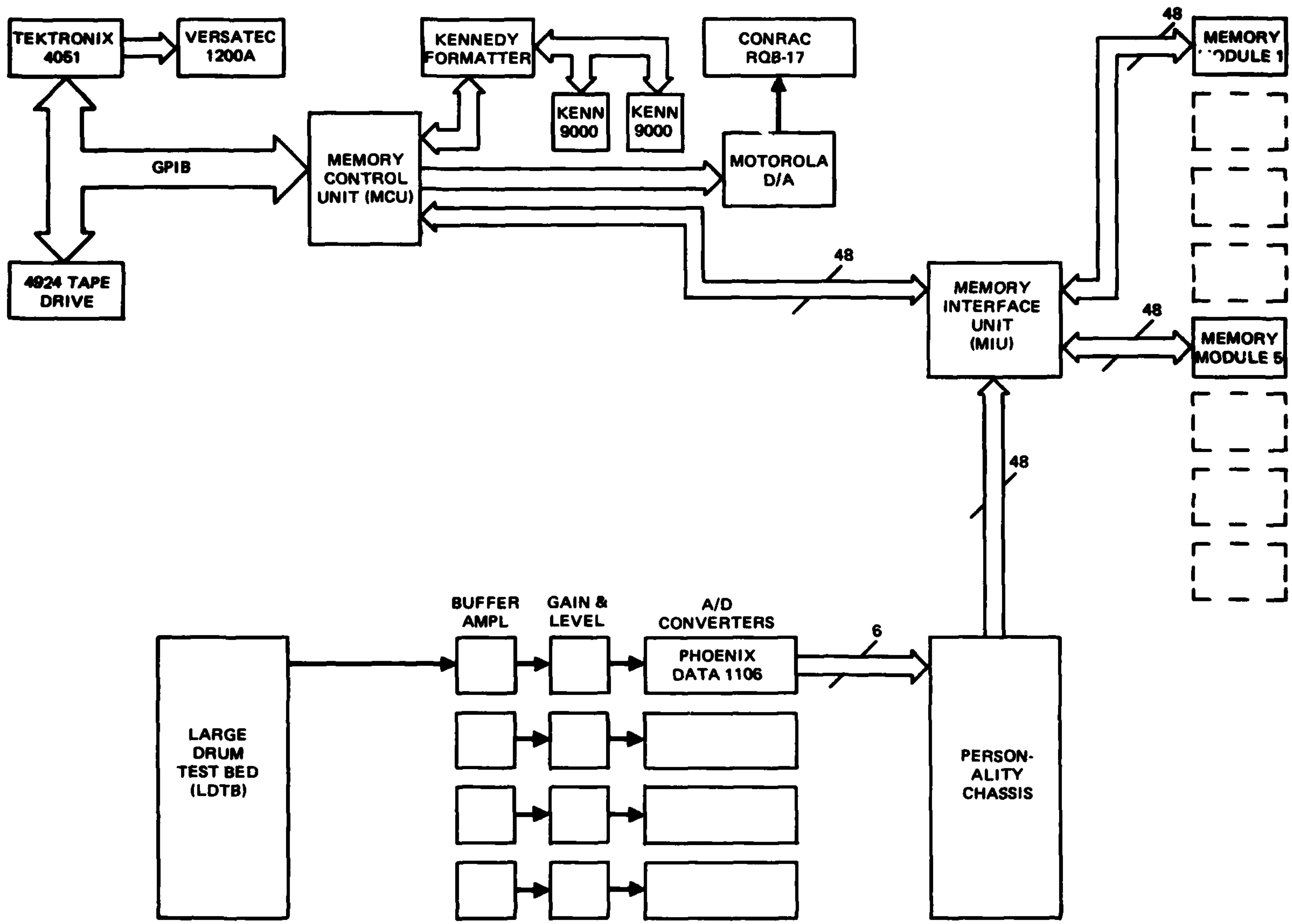


Figure D1. FY77 ICAS configuration.

satisfy the speed requirements of acquisition. Two 9-track tape decks were added to allow mass storage and simplified processing of images. A hard-copy unit was added to provide listings of programs and plots of statistical results obtained with the ICAS.

For image acquisition, a large drum test bed (LDTB) was constructed using a 40.96-inch-circumference drum and a shaft encoder for sync. The previously used Datel A/D converter, which operated to 10.5 megapels per second, was replaced by four Phoenix Data converters with sample rates up to 100 megapels per second.

Because of the requirement to handle a number of different imaging devices, a personality chassis (PC) was constructed to format data from any imager into a single standard format. For each new device to be tested, it would only be necessary to build a single card or card set to properly format the data generated.

In FY77 only two of the planned eight modules in the FSM were incorporated into ICAS. Noise problems in the MIU prohibited incorporating the other six modules.

FY80 CONFIGURATION

To overcome the noise problem, the MIU was redesigned and rebuilt with a new address and data distribution that enabled the use of the full page FSM (see fig D2). In addition, a hardware display control was added to replace the previously used microprogrammed display control.

For single-channel applications, the Phoenix Data A/D converters have been replaced by a TRW 8-bit, 21-MHz converter. Using this converter at 6-bits shows very favorable results (see ref 2).

Two new peripherals and a new interface to an old peripheral have been added. A Dicomed D47 color image recorder allows the production of high-quality hard copy of images on black and white or color transparency, negative, or Polaroid film. A Comtal Vision One color display system allows manipulation of 512-by-512-pel segments of images in monochrome or color with function and pseudocolor processing.

The MCU was provided with an interface to allow both high-quality printing of textual data via the Versatec's internal character generator and bilevel hard copy of images (single bit plane) via the plot option.

In order to increase the program storage capability of the ICAS (and consequently throughput), a Tektronix 4907 file manager was acquired for use by the 4051. The 4907 is also used for temporary and permanent data storage.

Currently in progress is the construction of an upgraded scanning system. This system includes an improved scanner table, new illumination source, and new analog preprocessing circuitry. The design is configured to allow simplified incorporation of new imaging devices.

ICAS OPERATION

Significant changes have been made in the operation of the ICAS, from both operational facility and operational capability points of view. The operational facility refers to the ease with which an operator may perform a given task or set of tasks using the ICAS. The operational capability refers to the number of different tasks which can be performed. The changes in capability have resulted primarily from an increase in the

2. Improved Technology Evaluation Report, by Lee A Wise, May 1980

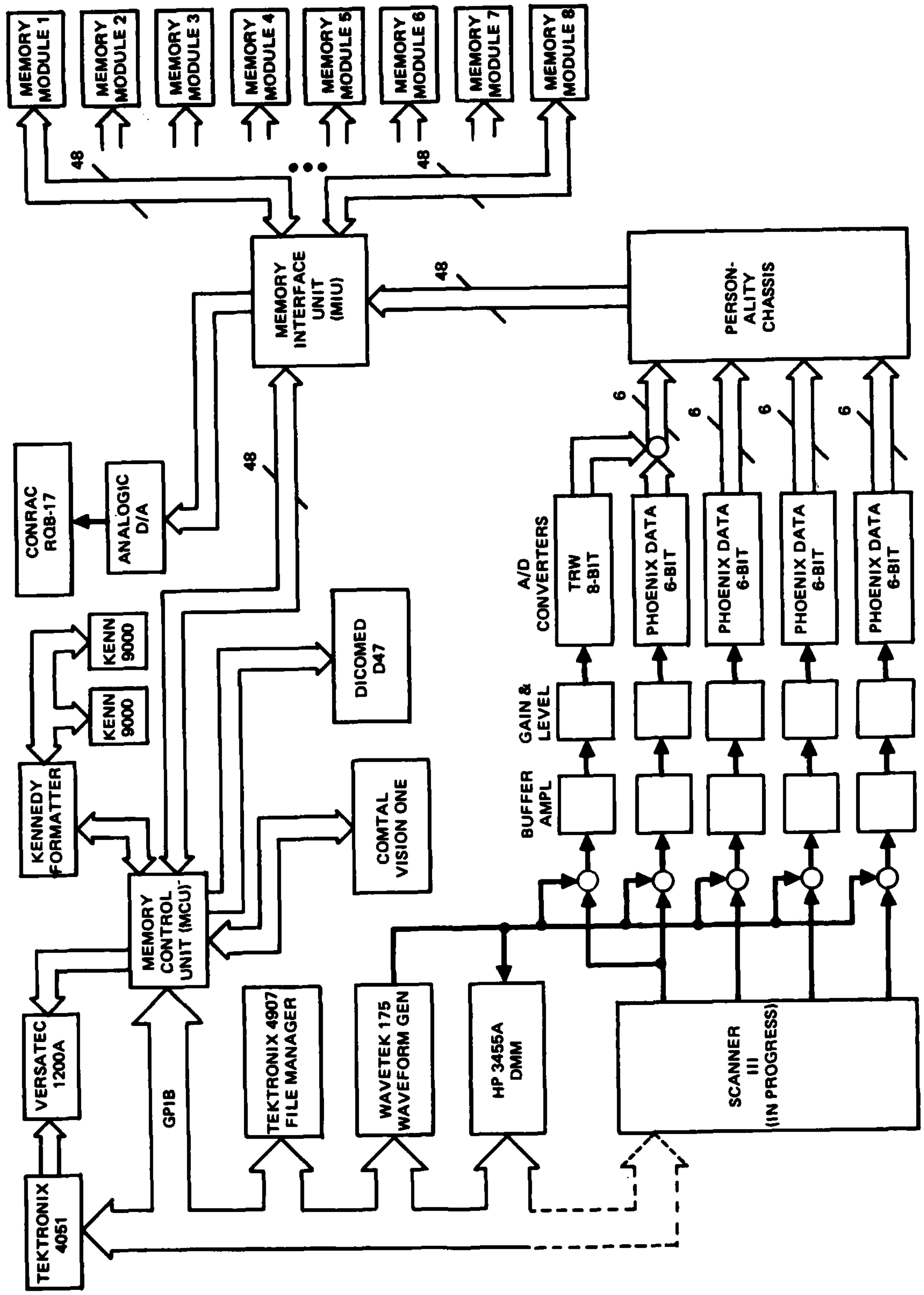


Figure D2. FY80 ICAS configuration.

available hardware and a consequent increase in the support software. Changes in facility were largely made possible by the acquisition of additional hardware but were motivated primarily by a desire to increase system throughput. This was accomplished by reducing the requirement for very detailed knowledge of the internal operation of hardware, thereby facilitating system operation.

DISK OPERATING SYSTEM (DOS)

As in FY77, in FY80 the ICAS is operated in a multiprocessing configuration, with the Tektronix 4051 serving as ICAS controller and the MCU serving as central processor and peripheral controller. The 4051 and the MCU are programmed with distinctly different yet complementary software, ensuring continuous, handshake-type communication. Software for the MCU is entered via the 4051 and may be stored on and retrieved from either of the nine-track tape drives. (For more detail see ref 1.)

In the FY77 configuration, software for the 4051 was stored in several groups on a magnetic tape cartridge and loaded into 4051 memory, one group at a time, as needed. This process was cumbersome and time-consuming and made software development awkward. With the introduction of the Tektronix 4907 file manager (January 1979), these problems were effectively eliminated. The software is organized in a multiple-overlay fashion to allow smaller blocks for faster access. This also saves memory space for data, allowing a reduction in the number of data transfers required for several operations. The addition of the 4907 has also reduced program development time through ease of access to the programs.

From a facility point of view, the DOS is designed to relieve the operator of the burden of knowing how the software performs its function. For efficient operation, a system should be designed so that all an operator needs to know is (1) a few simple rules of operational protocol and (2) what he wishes to accomplish. To this end, the DOS incorporates a number of aids for the operator's use. These aids include:

1. Extensive prompting. Whenever any data entry is required, a prompt is issued. When a command input is expected, the form of the prompt reflects the command grouping. When a parameter input is expected, the prompt specifically states what data quantity is required.

2. Extensive error checking. All commands and parameters entered are checked for legality and appropriateness. Any discrepancies with expected input are displayed immediately following the entry in order to provide immediate feedback. Error messages indicate the exact nature of the discrepancies.

3. Menus. Where multiple command selections are available, menus are available to assist the operator in selecting the desired function. In the basic command input mode, the command MENU allows access to brief descriptions of all other basic commands. After selection of a basic command, if an option entry is expected, a list of available options may be obtained by pressing a single key.

4. Graceful operation abort. At any time before the last parameter is entered for a given task to be performed, the operation may be aborted by a two-keystroke entry. This entry is the same for all command sequences.

From the point of view of capability, the DOS has simplified the addition of new tasks. The addition of a substantial amount of hardware has increased the number of tasks that can be performed. The FY77 configuration of ICAS supported 15 different commands (see table D1), most of which were quite primitive. An image capture required the operator to set individual switches on the MCU. In contrast, the DOS (FY80 configuration) consists of 55 basic commands (see table D2), several of which have a number of options.

RETURN	Retrieves the value of a specified memory location for display on the 4051
STORE	Saves a specified data value in a specified memory location
GOTO	Causes program execution in the MCU to switch from MONITOR to a special purpose program. When execution is complete, the program must return control to MONITOR
WRITE	Places on magnetic tape a single logical record consisting of the data occupying a specified block of memory locations
READ	Places in a specified location of memory the contents of a single logical record off magnetic tape
REWIND POSITION SBK SFK BBK BFK	A combination of these instructions positions magnetic tape unit at any desired location (file and record)
FILEMARK	Places a filemark on magnetic tape
MOVE	Transfers a block of data from one set of memory locations to another
DISPLAY	Displays a specified 440-line by 432-pel segment of an image from tape on a video monitor
SEARCH	Allows selective examination and modification of a block of memory based on a specified bit pattern

Table D1. Monitor command summary (FY77).

System parameter control	
ENV	Display set environmental parameters
BEL	Set prompt (DOS or auxiliary) tone length
MEN	Display command menus
Utility commands	
INS	Inspect and change memory locations
CNS	Store constant in block of memory
MOV	Copy block of memory to new location
SEA	Search memory for specified bit pattern
CMP	Compare two blocks of memory
TEX	Text transfer operations (disk, tape, memory)
SBK	Skip one physical block on tape
BBK	Backspace one physical block on tape
SFK	Skip one file on tape
BFK	Backspace one file on tape
POS	Position tape to specified file and record
REA	Read one physical block from tape
WRI	Write one physical block to tape
FIL	Write filemark on tape
DEN	Select tape density
MAR	Save three program banks on beginning of tape
LOA	Load three program banks from beginning of tape
VER	Verify record lengths in image file on tape
LIS	List programs to Versatec
Image acquisition	
CAP	Capture image
RES	Perform resolution verification on scanner
TAB	Generate illumination correction tables
STA	Generate white standard illumination curve
SMO	Smooth white standard illumination curve
Image display and hard copy	
DIS	Display image from tape or memory on CRT
ANN	Annotate image in refresh memory
COL	Color image processing (Comtal) operations
PRI	Print bilevel image on Versatec
D47	Color film recorder (Dicomed D47) operations
Image manipulation and processing	
FUN	Generation and manipulation of function tables
PRO	General image processing functions
COP	Copy image from tape to tape
SAV	Save image in memory on tape
THR	Perform Fairchild thresholding algorithm
ROT	Rotate image in memory (multiple of 90 deg)
MIN	Minify image in memory

Table D2. DOS command summary (FY80)

Image analysis and statistics use		
	MEA	Perform meander analysis on image
	ANA	General analysis functions (PBS, etc)
	SST	Save statistics on tape
	RLS	Output run length
	PBS	Output pel brightness statistics
	FDS	Output first difference statistics
	SFI	Output spatial identification statistics
	ILL	Plot illumination curve
	ARP	Array processing functions
	IMA	Plot image line(s)
	FFT	Perform operations on FFT data
	COM	Compression and compression ratios
Hardware test routines		
	ADT	A/D converter testing

Table D2. (Continued)

SOFTWARE MAINTENANCE

In addition to the improved operational aspects of the FY80 over the FY77 configuration, the software development and maintenance procedures have been greatly simplified, primarily by the establishment of a set of simple rules for the generation of new software, along with a set of maintenance programs designed to accommodate the rules. Basically, the rules govern the use of variables, selection of command names and program file names, and the interaction protocol between operator and terminal and between 4051 and MCU.

The primary maintenance program is the assembler for MCU software. Previously, all programs for the MCU were written in machine language, which was time-consuming and provided little or no documentation in and of itself. With the introduction of the assembler, initial program generation time was decreased by about 50%. The assembler is also largely self-documenting, which eases and speeds the debugging procedure and provides permanent documented descriptions of the intended operation. Figure D3 is a sample of an assembly listing. It is easily seen that the comments can simplify future modification by providing a fairly clear description of the intent of the program.

Other maintenance programs allow such things as updating of menus, updating of the list of commands that will be recognized by the DOS, and updating of the list of variable names that are recognized by the assembler.

DATA BASE CATALOG

Since the beginning of NOSC participation in the EMS program, a substantial library of digitized images has been acquired. In order to simplify the task of keeping track of both the images and statistical data for each of them, a data base catalog was designed and implemented. This catalog allows an individual entry to be made for each image or set of statistics on tape. The entries include the following information: document number, document class, image location (tape and file number), type of image (eg, scanning mode), statistics location (tape and file number), type of statistics (eg, PBS), and any supplementary information required.

```
ASSEMBLED CODE FOR SOURCE FILE:    C48X16          15-APR-80 10:01:08

LINE   ADDR     MACHINE CODE          SYMBOLIC CODE

  1  44400  2360000000000220   C48X16   JSR   RSDEC7       ;routine to generate a tape recor
  2  44401  2020000000044447            STA   NWRDS        ;   16-bit values from an array v
  3  44402  2360000000000222            JSR   RSDEC7+2
  4  44403  2020000000044450            STA   ADDR
  5  44404  2360000000000222            JSR   RSDEC7+2
  6  44405  2020000000044451            STA   FMF
  7  44406  2360000000003234            JSR   POSIT        ;position tape for output
  8  44407  2250000000044411            JPZ   *+2
  9  44410  2350000000000000            JPR                ;invalid tape location
 10  44411  2045000000044447            LDX   5,NWRDS      ;number of words counter
 11  44412  2044000000044450            LDX   4,ADDR       ;source data address pointer
 12  44413  2043000000044446            LDX   3,ADDRJ      ;destination address pointer
 13  44414  2042000000000773   LOOP     LDX   2,C3         ;source value/destination word co
 14  44415  2650000000000000            LDAC  0            ;initialize output word
 15  44416  2020000000044452            STA   TWRD
 16  44417  2014000000000000            LDAX  4,0          ;next value
 17  44420  2440000000044445            AND   MASK
 18  44421  2450000000044452            IOR   TWRD
 19  44422  2330000000000000            BYT
 20  44423  2330000000000000            BYT
 21  44424  2124000000000000            INX   4
 22  44425  2142000000000000            DSZ   2            ;check for output word complete
 23  44426  2200000000044416            JMP   LOOP+2
 24  44427  2033000000000000            STAX  3,0          ;save output word
 25  44430  2123000000000000            INX   3
  6  44431  2145000000000000            DSZ   5            ;check for done
  7  44432  2200000000044414            JMP   LOOP
 28  44433  2000000000044447            LDA   NWRDS        ;generate tape output instruction
 29  44434  2670000000000001            SUBC  1
 30  44435  2420000000000030            SLZ   24
 31  44436  2500000000044446            ADD   ADDRJ
 32  44437  2450000000000725            IOR   OP2746
 33  44440  2360000000004100            JSR   WRREC
 34  44441  2000000000044451            LDA   FMF
 35  44442  2250000000044444            JPZ   *+2
 36  44443  2360000000001221            JSR   FILMRK+1
 37  44444  2350000000000000            JPR
 38                                ;
 39                                ;VARIABLES AND CONSTANTS
 40  44445  0000000000177777   MASK     0177777            ;16-bit mask
 41  44446  0000000001770000   ADDRJ    01770000           ;output buffer address
 42  44447  0000000000000000   NWRDS    0                  ;number of output words
 43  44450  0000000000000000   ADDR     0                  ;address of first source value
 44  44451  0000000000000000   FMF      0                  ;filemark flag
 45  44452  0000000000000000   TWRD     0                  ;temporary output word
```

Figure D3. Sample of assembly listing.

In addition, the catalog software allows the selective retrieval and listing of portions of the catalog. Sequential listings may be obtained in either document number or tape and file location order. For example, if it is desired to determine which tape and file contains document three acquired in prescan mode, a list is generated for document three only, and the required entry is selected. This procedure eliminates the necessity of a search through written records to locate a particular image or statistical data file. Figure D4 is an example of a search for all references to images of documents in class 2.

The catalog also maintains a list of all documents currently in the data base. Figure D5 is a portion of the current list.

FIRMWARE MEMORY TEST

In a semiconductor memory as large as that in ICAS, an occasional failure is to be expected. The most common failure is the demise of a single memory chip. This type of failure is usually characterized by a failure of software to operate correctly or by "holes" in an image in refresh memory which are visible on a display monitor. This type of failure may also (usually) be isolated and remedied quickly.

Occasionally, a single bit within a single memory chip will fail. This type of failure may go unnoticed for a long period of time, especially if it is located so that no obvious errors in results ever occur. Previously, numerous software programs had been written (for the ICAS) which were intended to detect both single- and multiple-bit failures. These programs had two disadvantages, however. These were:

1. They were very slow. Testing a single pattern in each of the 512k words of memory requires a minimum of about 24 seconds. For a 48-bit word, a minimum of 100 patterns are required (all ones, all zeros, alternating zeros and ones, alternating ones and zeros, walking one and walking zero). The total time required for all 100 patterns is about 40 minutes.

2. They required memory space. The programs to test memory were required to reside in the memory being tested. This meant relocatable code was required. In addition, if the failure was massive, the software might not work at all.

In order to overcome these problems, a memory test was programmed in firmware. The memory test firmware is currently programmed into relatively slow (2 μs) PROMs, but still cuts complete test time to about 30 minutes. The test could be transferred into high-speed (500-ns) PROMs, allowing a further reduction to about 7 1/2 minutes for all 100 patterns. The fact that the test program does not reside in the main random access memory (RAM) to be tested means that no relocation is required and that the test will always operate, regardless of the amount of memory affected by the failure.

The firmware test has to date detected a number of single-bit errors which might have gone unnoticed otherwise. This permits a higher degree of confidence in results, as the test may be run frequently and easily.

DATA FILES CATALOGUED AS OF 24-JUL-8Ø 12:Ø7:22

SERIAL	CLASS-NUMBER	IMAGE TYPE	IMAGE TAPE/FILE	STATS TYPE	STATS TAPE/FILE	DESCRIPTION
WJM typed page						
1	2 1	PU	52 2			
17Ø	2 1	PCS	67 9			
261	2 1	PC	67 8			
3Ø1	2 1	PC	68 Ø			WJM typed page 52/2 ill corrected 275 lines
3Ø2	2 1	T	68 1			Test image - PC : PCS : PC xor PCS
3Ø3	2 1	T	68 2			PC : PCS : PC xor PCS - comp. - 6 bit planes
3Ø4	2 1	T	68 3			6-bit version of composite on 68/Ø2
3Ø7	2 1	T	68 6			6 bit plane composite with recursive filter
3Ø8	2 1	T	68 7			6-bit version of composite on 68/Ø6
311	2 1	PCR	68 1Ø			
46Ø	2 1	PU	78 7			Mux'ed outputs - 8.5" leading - 4 pps
461	2 1	PU	78 8			Mux'ed outputs - 11" leading - 4 pps
472	2 1	PC	79 9			Mux'ed outputs - 8.5" leading - 4 pps
476	2 1	PC	79 13			Mux'ed outputs - 11" leading - 4 pps
WJM typed page (increased PCR)						
24	2 2	PU	55 4			
ACCUPRESS typed page 1						
1Ø4	2 3	PU	62 1Ø			
ACCUPRESS typed page 2						
124	2 4	PU	63 14			

Figure D4. Sample data base list.

DATA BASE DOCUMENTS CATALOGUED AS OF 28-JUL-80 10:28:57

SERIAL	CLASS-NUMBER		DESCRIPTION
1	1	1	BRUNING typed page
2	1	2	DATA COMMUNICATIONS typed page
3	1	3	USN & WR typed page
4	1	4	DYNASALES typed page
5	1	5	IIR SAMPLE typed page
6	1	6	GROSSBOHLIN letter typed page
7	2	1	WJM typed page
8	2	2	WJM typed page (increased PCR)
9	2	3	ACCUPRESS typed page 1
10	2	4	ACCUPRESS typed page 2
11	2	5	CREDIT UNION typed page
12	2	6	OPTICAL SOCIETY typed page
13	2	7	USN & WR typed page
14	2	8	POSTAL BULLETIN typed page
15	3	1	GWU typed page
16	3	2	USPS HQ ANNOUNCEMENT typed page
17	3	3	LAW typed page
18	3	4	CORNING ADVERTISEMENT typed page
19	3	5	WEC typed page
20	3	6	MDF, LTD typed page
21	3	7	ORCO typed page
22	3	8	TRADING POST typed page
23	3	9	USPS - POSTAL BULLETIN typed page
24	3	10	ADVANCED DIGITAL GROUP typed page
25	3	11	HQ ANNOUNCEMENT typed page 2
26	3	12	ELECTRONIC PRODUCTS MAG. LETTER typed page
27	4	1	WTM typed page
28	4	2	GOULD typed page
29	4	3	VARIAN typed page
30	4	4	FRANKLIN ELECT. typed page
31	4	5	MUPAC typed page
32	4	6	FLOATING POINT typed page
33	4	7	GORE typed page
34	4	8	ELECTRONICS MAG. typed page
35	4	9	TEKTRONIX typed page
36	4	10	PLASTIGLIDE typed page
37	4	11	OPTO 22 typed page

Figure D5. Sample document list.

MCU PERIPHERALS

Since FY77, three new devices have been incorporated into the ICAS for purposes of image manipulation:

1. A Versatec 1200A printer/plotter
2. A Dicomed D47 color image recorder
3. A Comtal color image processing system

The use of these devices permits hard-copy output of images in two forms and permits investigations into color imaging characteristics. This indicates a greatly increased ability to meet future processing requirements. Figures D6 and D7 show the FY77 and FY80 MCU configurations.

VERSATEC 1200A PRINTER/PLOTTER

This device had been incorporated into the ICAS in the FY77 configuration; however, its use was limited to the production of hard copies of the display on the 4051. In order to allow generation of hard copies of acquired images, a parallel interface was designed and implemented in the MCU for the 1200A. This interface also allows the 1200A to be used as a line printer by way of its internal character generator.

The MCU interface for the 1200A consists of an 8-bit data output port, a 7-bit command output port, a pel clock output, and three status input lines. The data lines carry either 1-bit pels in parallel or a single alphanumeric (ASCII) character, depending upon the operating mode. The seven command lines allow the operating mode to be set for alphanumeric print, image plot, or simultaneous print/plot. The simultaneous mode allows annotation of images or graphs being plotted.

DICOMED D47 COLOR IMAGE RECORDER

The D47 gives ICAS the capability of generating high-quality photographic output on several media. The media available include 35-mm and 101-by-127 mm (4-by-5 inch) transparency and negative film and 101-by-127 mm Polaroid print film, all in either black and white or color. Resolution on the film (subject to limitations of the individual film type) is 48 pels per mm (1210 pels per inch). Maximum printed image size is 4096 pels or 86-by-86 mm (3.38-by-3.38 inches) square.

The D47 has a number of operating mode options including 6-bit/8-bit selection, complement, logarithmic intensity, and four filters (red, green, blue, neutral). All operating modes are programmable via the interface.

The D47 interface in the MCU consists of an 8-bit image data/command output port, an 8-bit status input port, and three output and three input handshake control lines. The handshake lines are I/O request, I/O acknowledge, and I/O tag for differentiation between command and data.

COMTAL COLOR IMAGE PROCESSING SYSTEM

With increasing interest in the implications of scanning color documents, USPS decided to incorporate a color image display/processing system into the ICAS. Because of its extensive capability, the Comtal Vision One was chosen for this purpose. The Vision One is able to display monochrome or true color images. Additional features include function tables, pseudocolor processing, and graphic overlays. This equipment allows a display of the effects of tricolor separation scanning as well as manipulation of the recombined color components.

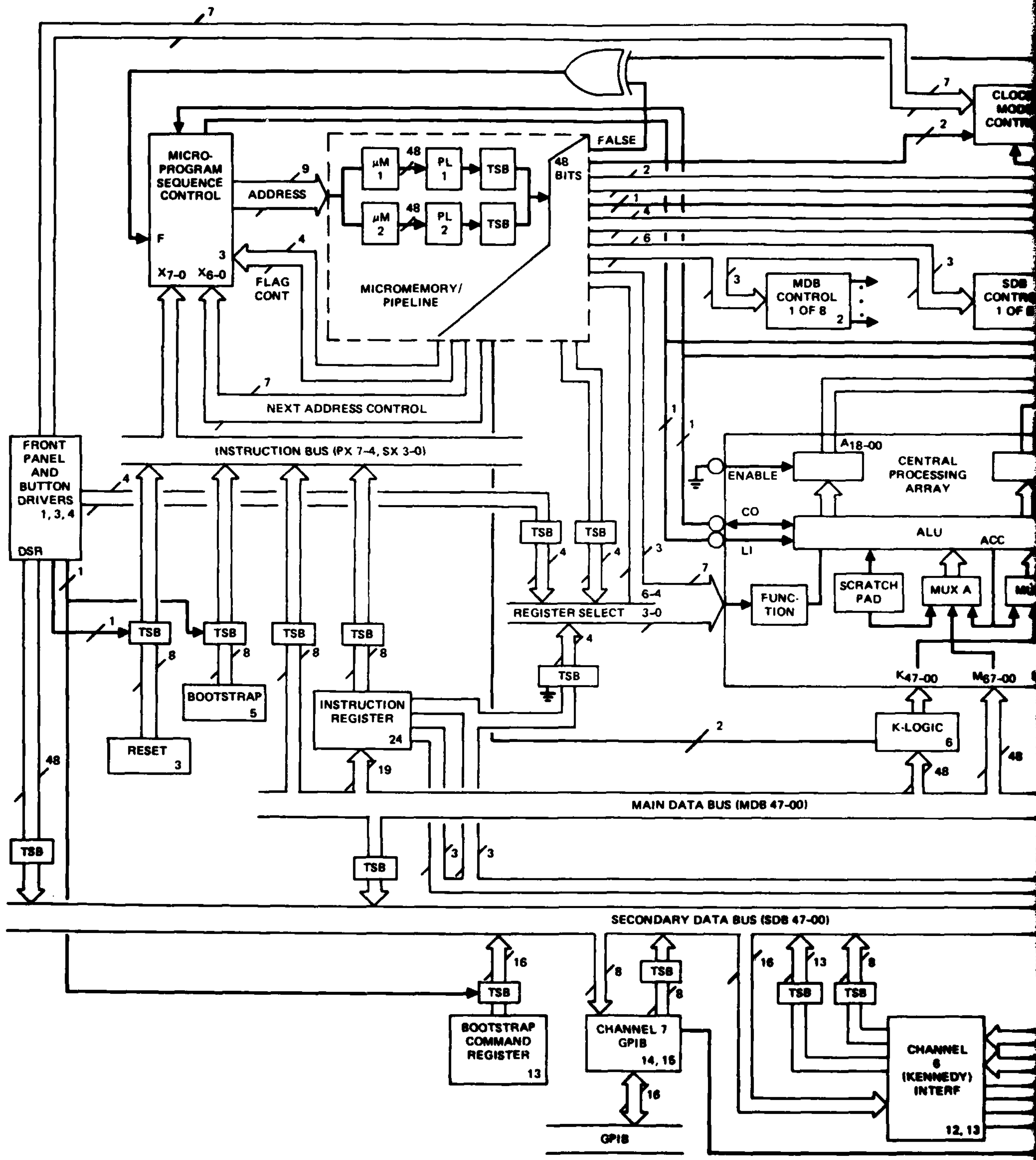
The Vision One interfaces available are for standard host computers such as the PDP-11. It was therefore necessary to design both interfaces at NOSC. However, the MCU interface in the Vision One consists primarily of a set of differential transceivers with a modest amount of control logic making the design quite straightforward. The Vision One interface in the MCU consists of a 16-bit bidirectional (balanced differential) bus used for both commands and data, six control output signals, and six control input signals. Operation is by handshake on a word-by-word basis.

FRAME-STORE MEMORY AND MIU-2

When two FSM modules were made operational with the first version of the Memory Interface Unit (MIU-1), about a 20% reduction was realized in the data transfer rate between memory and the MCU. This is due to additional logic in the control, address, and data paths in the MIU, and was fully expected. One adverse effect of this slower transfer rate was decreased ability of the MCU to support a reasonable refresh rate to the CRT monitor. It was then decided to design an additional function for the MIU, which was a DMA refresh display. The version 2 display, which is essentially the same as version 1 with a couple of added features, is described below. MIU-1, described in reference 1, was made operational with up to two memory modules. When an attempt was made to power up four memory modules at one time, several problems were encountered which prevented reliable system operation. First, there was excessive noise on address and data signal lines throughout the MIU. Second, there was an insufficient power level on the eight memory interface cards (MICs). Analysis of these problems showed that three steps were required to alleviate them.

The first two steps resulted in a need to actually fabricate a second MIU chassis, MIU-2. The first step involved a new backplane layout. MIU-1 contained several bundles of backplane wiring; ie, many parallel wires in very close proximity. This resulted in excessive levels of crosstalk between signal conductors. In order to remedy this, the control cards in the MIU had to be rewired to bring the signals out on different 1/0 pins corresponding roughly to the 1/0 pattern on the eight MIC boards, which are PC boards and not easily alterable. Thus, the new backplane contains no bundles of wires, which minimizes crosstalk. The second step was to break the 48-bit bidirectional data bus into two electrically separate buses. Originally this data bus was connected to all eight MIC cards and two control cards, which resulted in very long wire lengths, some in excess of 24 inches. As a general rule, TTL signals should not propagate more than 18 inches. The data bus was broken up into three separate buses by the introduction of a new circuit board called the bus switch card. From this card, there are two buses each of which connects to four of the MIC cards and one bus that connects to the two control cards and also to the new display card.

Close analysis of the eight MIC cards revealed the cause of the insufficient power levels on the cards. The problem was that choke points existed in the printed circuit etch which distributed power and ground to the ICs on the board. A number of 12 AWG jumper wires soldered in place on the boards solved the problem.



MICRO-PROGRAM SEQUENCE CONTROL
ADDRESS
F
X7-0 X6-0
FLAG CONT
μM 1
μM 2
PL 1
PL 2
TSB
48 BITS
FALSE
MICROMEMORY/ PIPELINE
NEXT ADDRESS CONTROL
INSTRUCTION BUS (PX 7-4, SX 3-0)
FRONT PANEL AND BUTTON DRIVERS 1, 3, 4
DSR
BOOTSTRAP 5
RESET 3
INSTRUCTION REGISTER 24
REGISTER SELECT
CLOCK MODE CONTR
MDB CONTROL 1 OF 8
SDB CONTR 1 OF 8
CENTRAL PROCESSING ARRAY
ENABLE
CO
LI
ALU
ACC
FUNC-TION
SCRATCH PAD
MUX A
K-LOGIC 6
MAIN DATA BUS (MDB 47-00)
SECONDARY DATA BUS (SDB 47-00)
BOOTSTRAP COMMAND REGISTER 13
CHANNEL 7 GPIB 14, 15
GPIB
CHANNEL 6 (KENNEDY) INTERF 12, 13

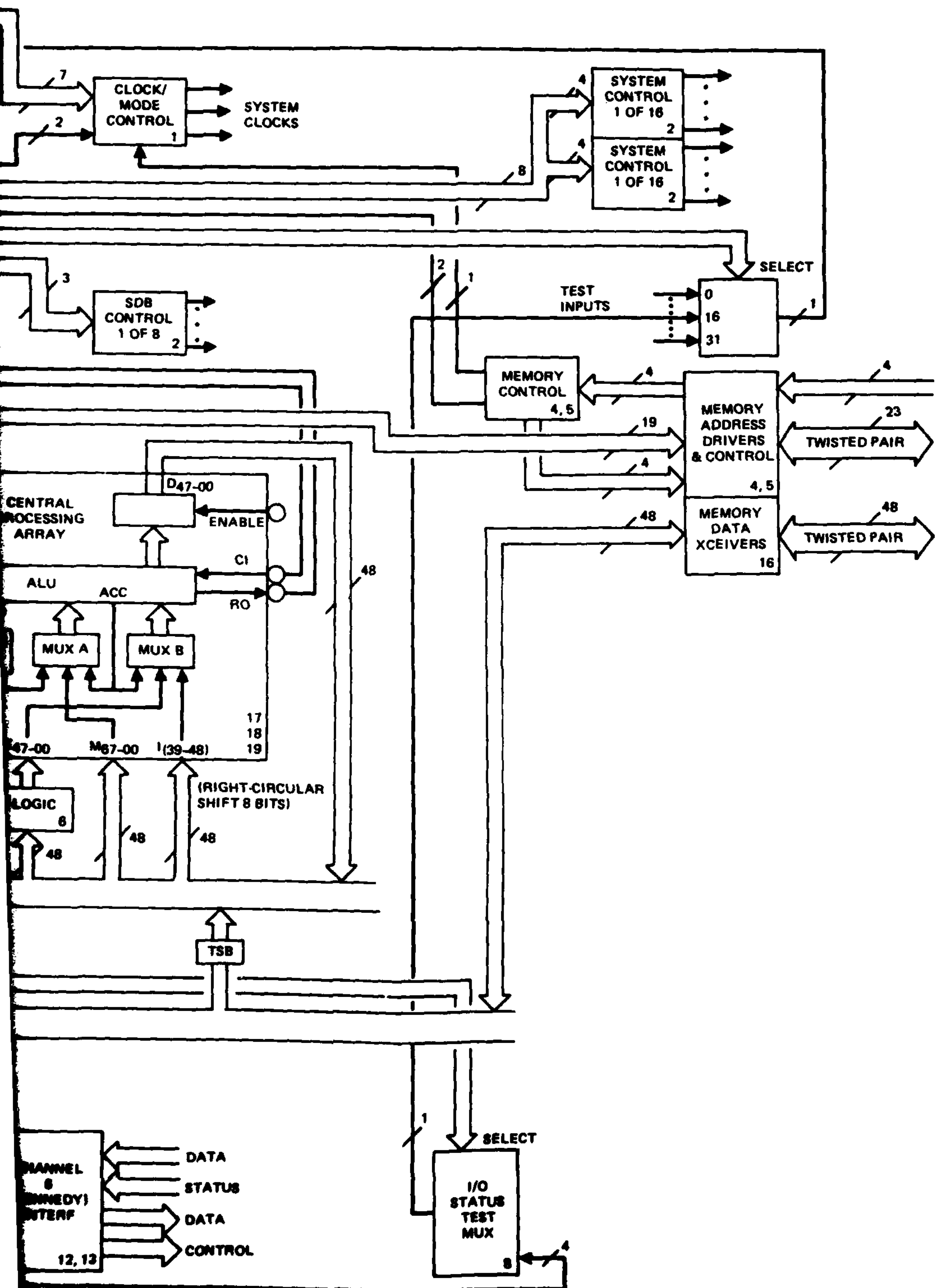
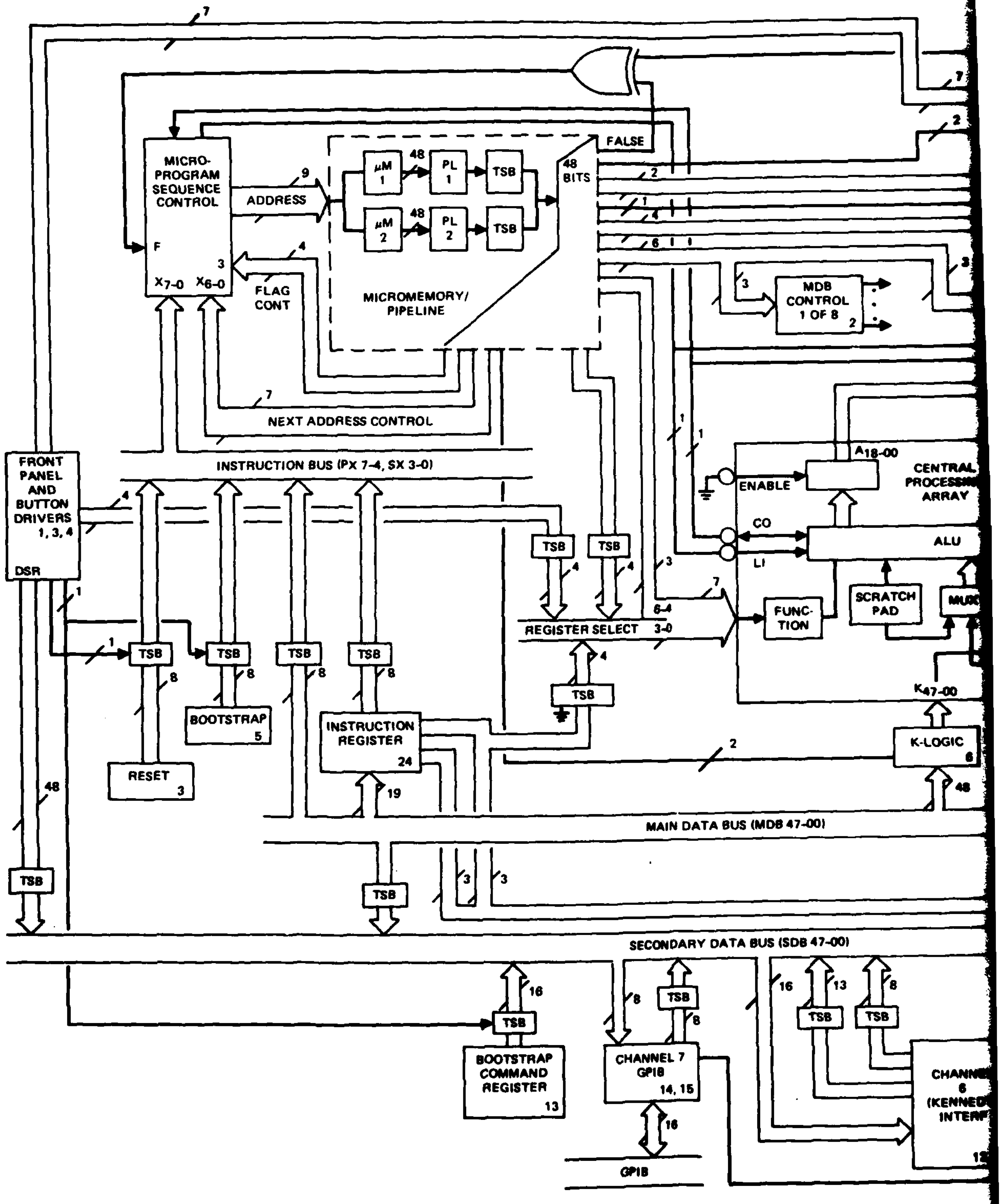


Figure D6. FY77 MCU configuration.


MICRO-PROGRAM SEQUENCE CONTROL
F
X7-0
X6-0
ADDRESS
FLAG CONT
μM 1
μM 2
PL 1
PL 2
TSB
48 BITS
FALSE
MICROMEMORY/ PIPELINE
NEXT ADDRESS CONTROL
MDB CONTROL 1 OF 8
INSTRUCTION BUS (PX 7-4, SX 3-0)
FRONT PANEL AND BUTTON DRIVERS 1, 3, 4
DSR
REGISTER SELECT
BOOTSTRAP 5
RESET 3
INSTRUCTION REGISTER 24
ENABLE
CO
LI
ALU
FUNCTION
SCRATCH PAD
K-LOGIC 6
MAIN DATA BUS (MDB 47-00)
SECONDARY DATA BUS (SDB 47-00)
BOOTSTRAP COMMAND REGISTER 13
CHANNEL 7 GPIB 14, 15
GPIB

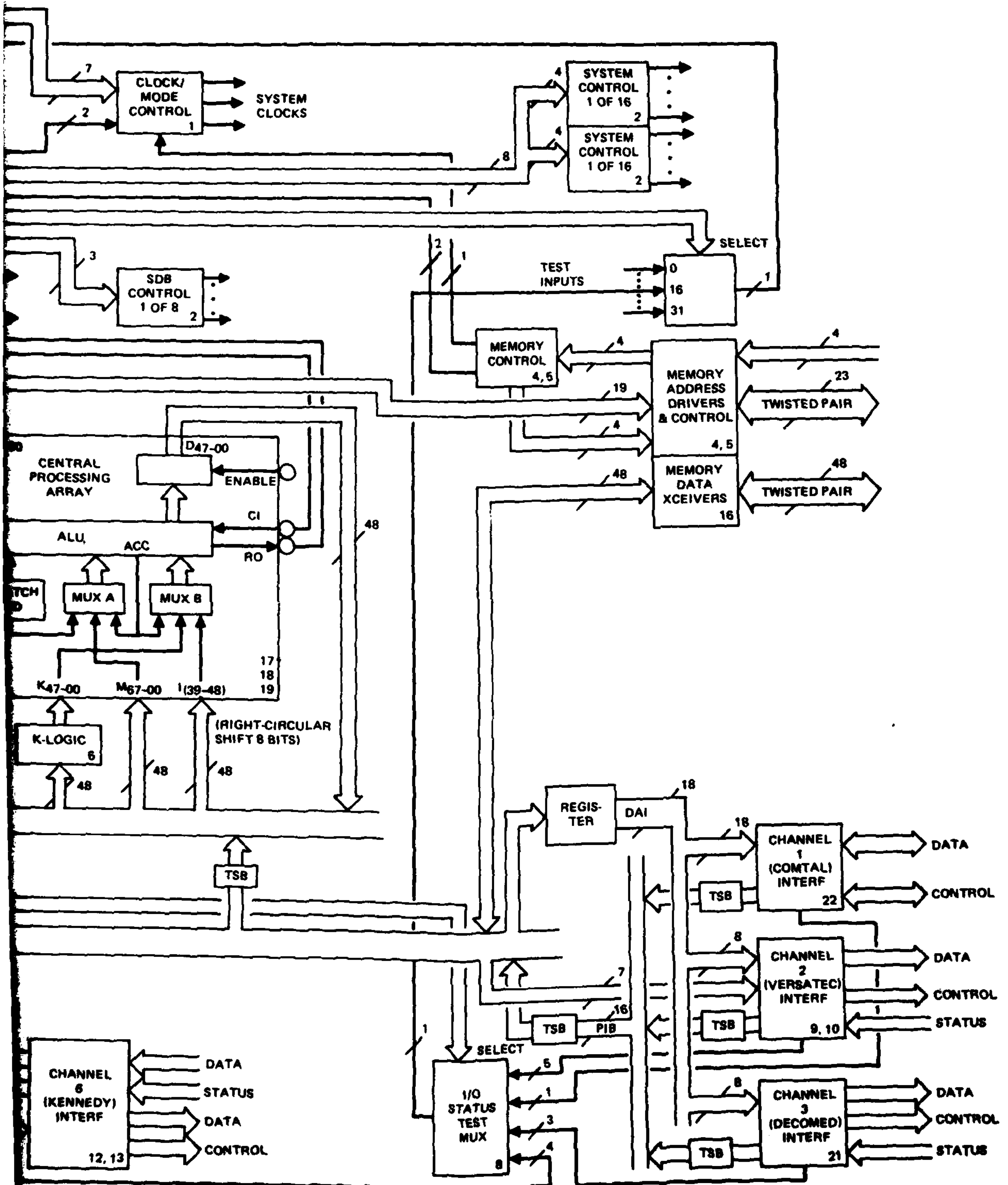


Figure D7. FY80 MCU configuration.

2

DUAL 48-BIT DATA BUS

A block diagram of the MIU-2 is shown in figure D8. This figure shows only memory data and address paths and how the buses are organized within the unit. The 48-bit data bus that in version 1 connected all eight MIC cards together has been split into data bus A and data bus B, each connecting only four MIC cards together. This cuts down the physical wire length and consequently the noise levels on these signals. The data bus switch card acts as a bidirectional switch to allow data coming from FSM modules 1-4 onto the multiplexed data bus (MDB) or data from modules 5-8 onto the MDB when data are read from memory. For data being written into memory, the data bus switch routes data from the MDB onto both data bus A and data bus B. A write command is then given to only the module into which the data are to be written.

The one other destination on the MDB is the display control card, which reads data from the FSM in a DMA mode in order to support a 9.45-MHz pel rate for the CRT display.

DMA IMAGE CAPTURE

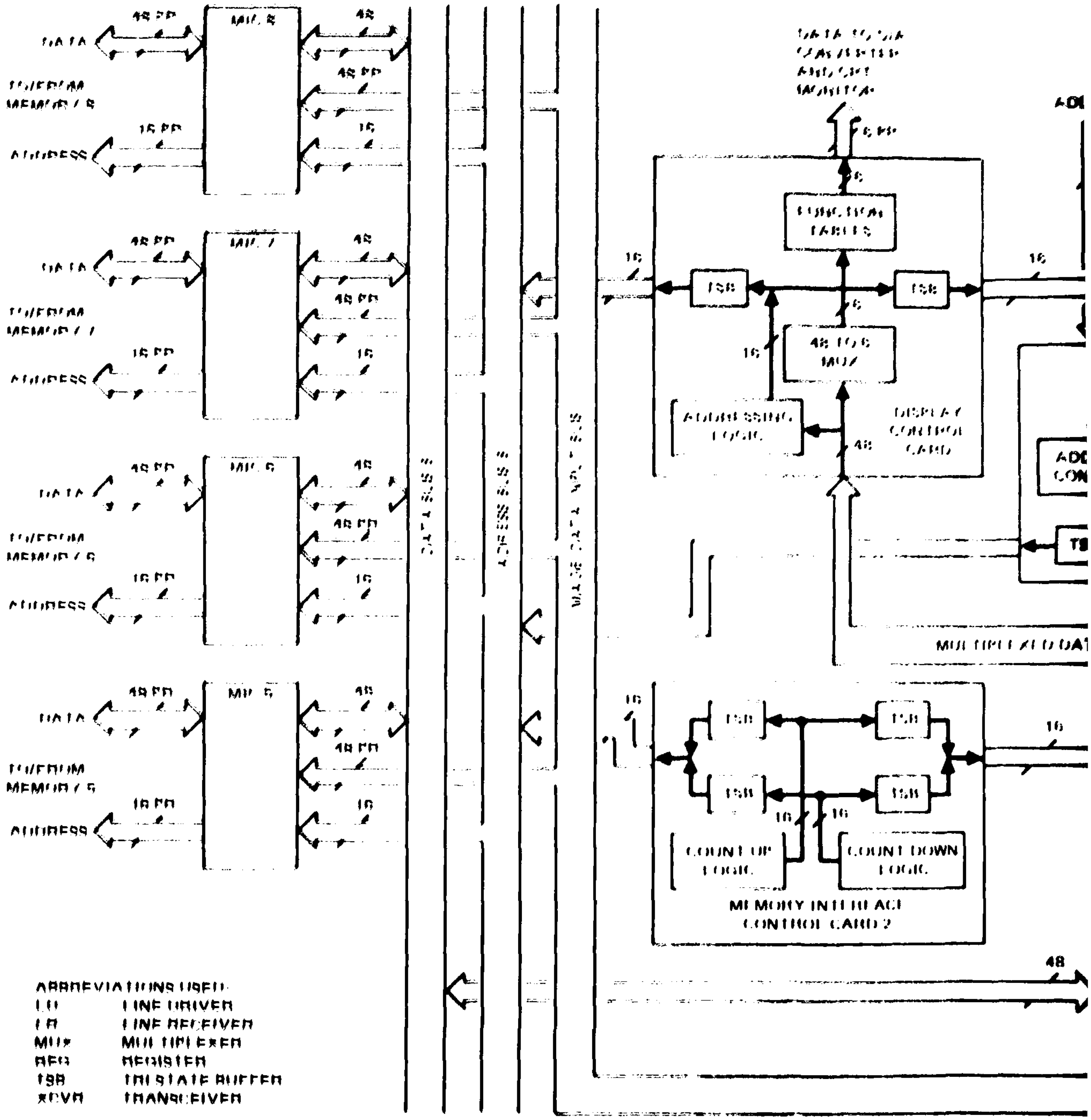
For image capture, data from the personality chassis (PC), which have been formatted into 48-bit words, are input to the image data input bus. This bus is common to all eight MIC cards. Memory interface control card 2 (MICC-2) contains the address generation logic for image capture in any of several image formats. Memory interface control card 1 (MICC-1) contains the control logic necessary to store the 48-bit words into the appropriate MIC card scanner data register. During a capture sequence, control logic in the MIU completely inhibits the MCU from performing any memory transfers until the capture process is completed; hence, the term direct memory access. This operation, explained in more detail in reference 1, has not changed with the addition of MIU-2.

DISPLAY CONTROL HARDWARE

The display control hardware provides a 496-pel, 482-line display on the Conrac RQB monitor in a standard 525-line television format. It performs this function using a DMA read mode during the active line time and allowing the MCU access to the FSM during retrace times. The horizontal and vertical retrace times account for about 20% of a frame time; thus, the MCU processing speed while the display function is enabled is about 20% of maximum.

Figure D9 is a block diagram of the display control card. Only the data path and the memory address control circuitry are shown.

In order to dynamically "roam" around a 1700-by-2200 pel image in memory, a means had to be provided for the MCU to alter the starting coordinates of the display window. Two registers are provided which contain starting addresses for field 1 and field 2. These absolute memory addresses must be calculated in either the 4051 terminal or the MCU and loaded into these control registers either before the display function is activated or during display, since the MCU does have limited-speed processing capability. To provide a proper 2:1 interlaced display, the addressing must be done in a unique manner, illustrated in figure D10. During one field time every other image line is painted on the CRT for a total of 241 lines. For example, during field 1 lines 1,3,5,... are displayed. To accomplish this, the starting address for field 1 must be used for reaching the first eight pels from memory, and thus incremented for the next eight pels, etc, until the end of the displayed line is reached. Then


DATA
ADDRESS
48 PP
16 PP
48
16
DATA BUS
ADDRESS BUS
FUNCTION TABLES
TSB
48 TO 6 MUX
ADDRESSING LOGIC
DISPLAY CONTROL CARD
MULTIPLEXED DATA
COUNT UP LOGIC
COUNT DOWN LOGIC
MEMORY INTERFACE CONTROL CARD 2
ABBREVIATIONS USED:
LD LINE DRIVER
LR LINE RECEIVER
MUX MULTIPLEXER
REG REGISTER
TSB TRISTATE BUFFER
XCVR TRANSCEIVER

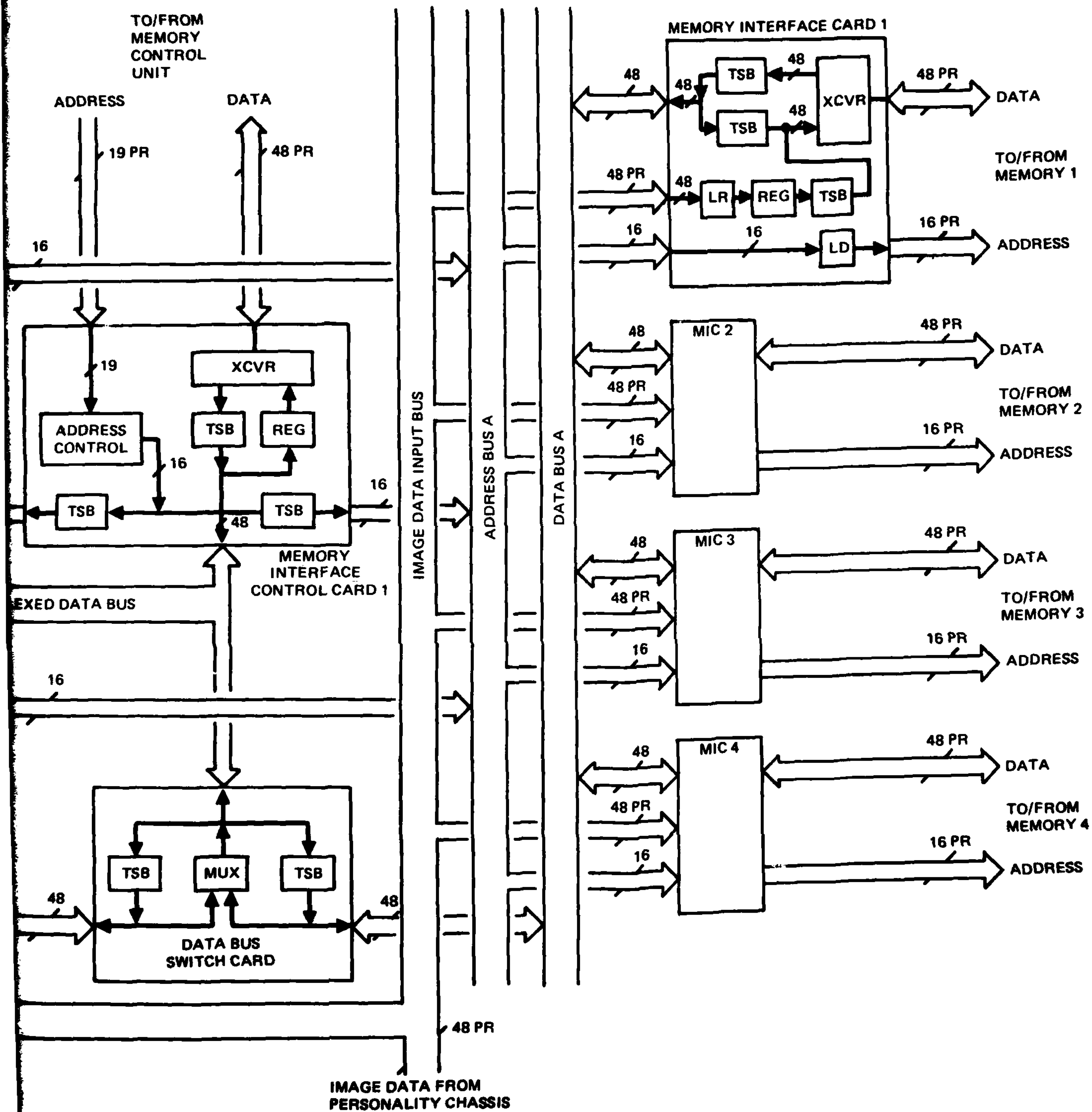
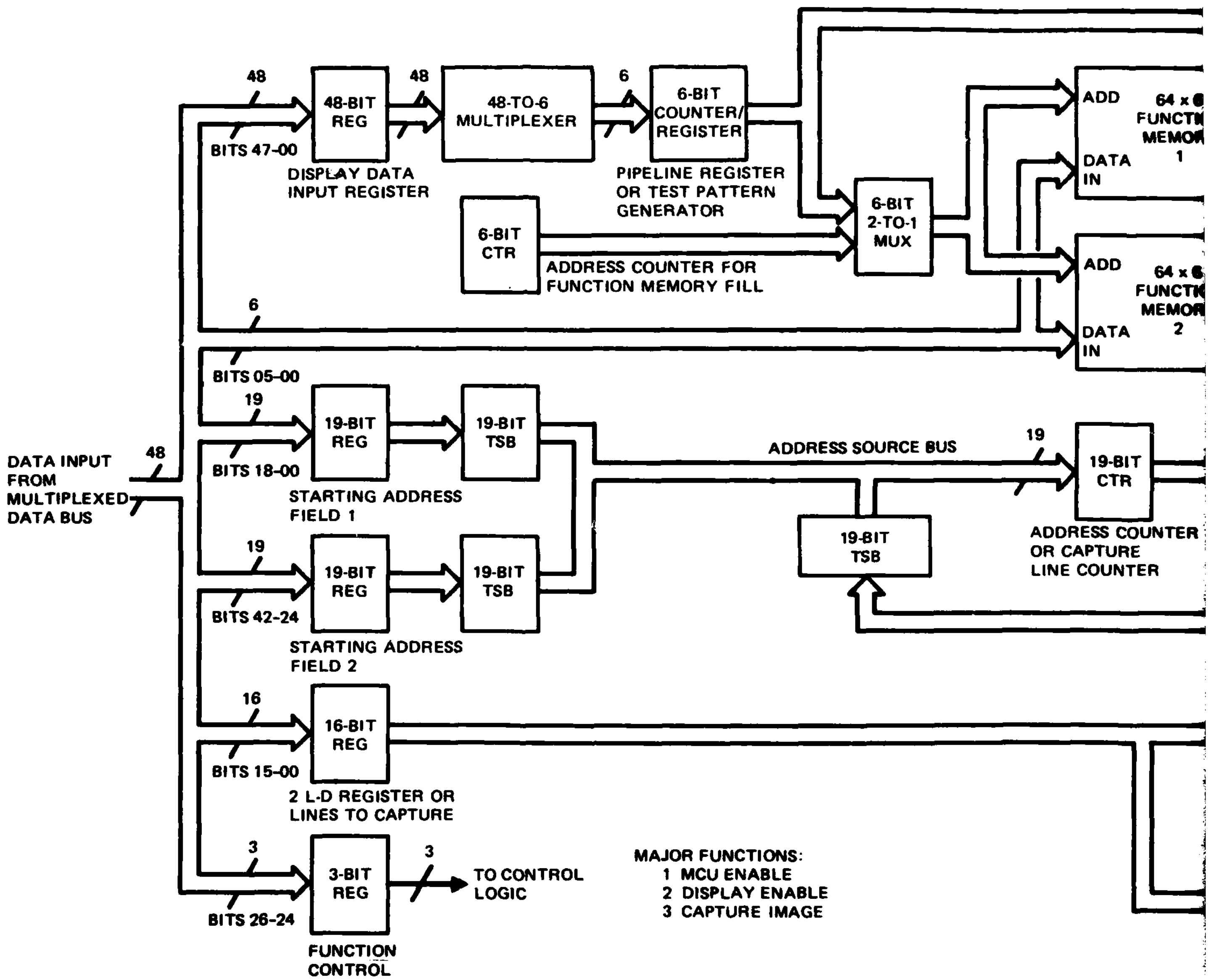


Figure D8. Memory interface unit.



48
48-BIT REG
BITS 47-00
DISPLAY DATA INPUT REGISTER
48
48-TO-6 MULTIPLEXER
6
6-BIT COUNTER/ REGISTER
PIPELINE REGISTER OR TEST PATTERN GENERATOR
6-BIT CTR
ADDRESS COUNTER FOR FUNCTION MEMORY FILL
6-BIT 2-TO-1 MUX
ADD
DATA IN
1
ADD
DATA IN
2
6
BITS 05-00
19
19-BIT REG
BITS 18-00
19-BIT TSB
STARTING ADDRESS FIELD 1
ADDRESS SOURCE BUS
19
19-BIT CTR
ADDRESS COUNTER OR CAPTURE LINE COUNTER
19-BIT TSB
DATA INPUT FROM MULTIPLEXED DATA BUS
48
19
19-BIT REG
BITS 42-24
19-BIT TSB
STARTING ADDRESS FIELD 2
16
16-BIT REG
BITS 15-00
2 L-D REGISTER OR LINES TO CAPTURE
3
3-BIT REG
BITS 26-24
FUNCTION CONTROL
3
TO CONTROL LOGIC
MAJOR FUNCTIONS:
1 MCU ENABLE
2 DISPLAY ENABLE
3 CAPTURE IMAGE

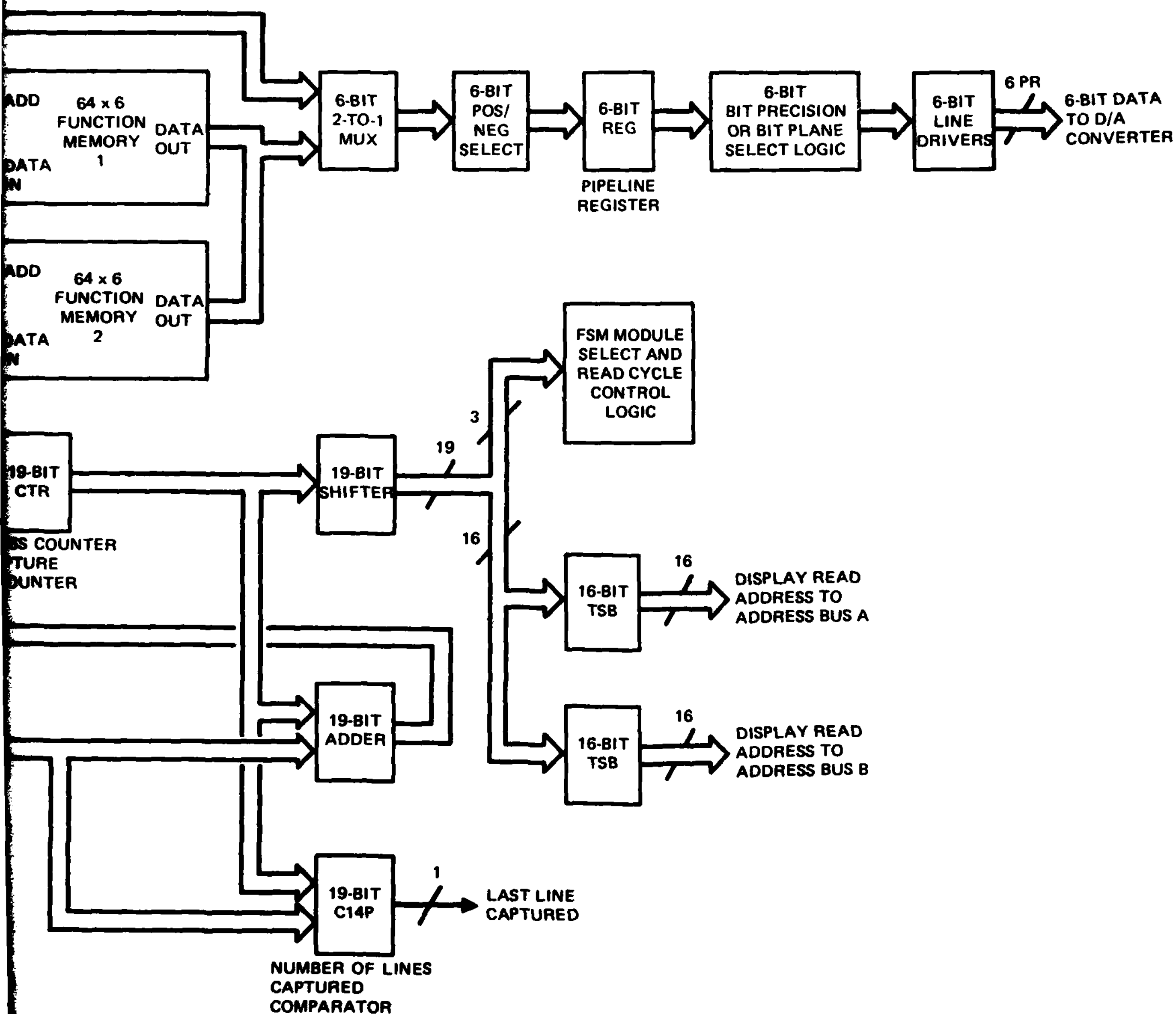


Figure D9. Display control card block diagram.

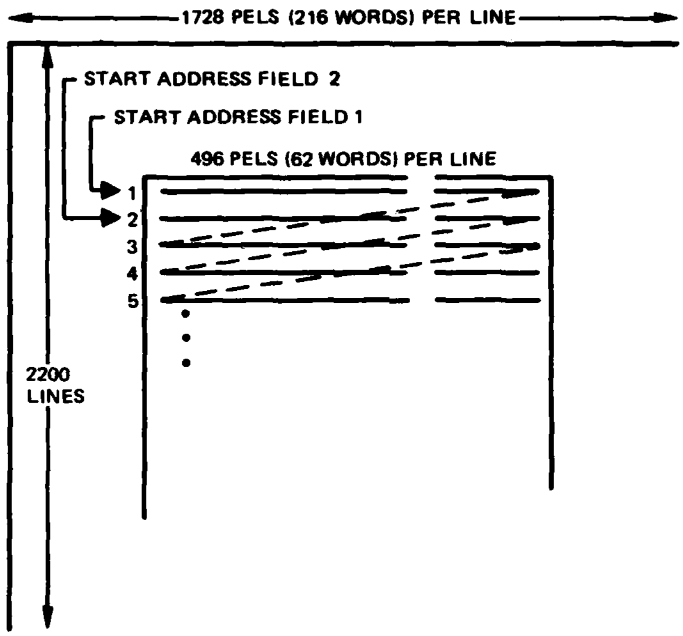


Figure D10. Memory addressing sequence for display refresh.

some increment must be added to the last address to get from the end of line 1 to the beginning of line 3. For the normal case in ICAS an image in memory is 1728 pels (or 216 words) per line by 2200 lines. However, a line displayed on the CRT is only 496 pels (or 62 words) long. If L is number of words per line in frame-store memory, and D is number of words displayed per line, then adding 2L-D to the last address on one line provides the starting address for the next line to be displayed in that field. Referring to figure D9, three registers are used to define the display coordinates, starting address field 1, starting address field 2, and 2L-D.

During the display cycle, the starting address for the field to be scanned is loaded into the address counter via the address source bus, which is then incremented while the first line is scanned. At the end of the first and all succeeding lines, the contents of the 2L-D register are added to the current contents of the address counter and the result is then loaded into the address counter via the address source bus. The blocks labeled TSB are tristate buffers used to selectively enable different sources onto a common data bus.

The output of the address counter then goes through a 19-bit shifter which allows for reduced operation of ICAS with four, two, or one memory module. From the shifter the three least significant bits of the 19-bit address are used as a memory module select while the other 16 bits are output to each of the eight modules via the two address buses.

One additional function performed in the address generation logic is that of controlling the number of lines captured during image acquisition. The number of lines to be captured is stored in the same register used for the 2L-D constant. The address counter is cleared, then incremented, as image lines are stored in the FSM. A comparator compares the counter output with the number of lines to be captured and generates an output (the last line captured signal) which is used by the control circuitry.

The data path through the display control card begins with the 48-bit data input register at the top of figure D9. 48-bit words are read from memory at the rate of 1.18 MHz. From this register the data are multiplexed down to a 6-bit pel channel operating at a 9.45-MHz rate. The pipeline register at the output of the multiplexer can also be used as a test pattern generator for verification of system operation. From this point image data may optionally be sent to one of two function memories. Each function memory consists of 64 words by 6 bits and is loaded directly from the 48-bit data bus under MCU control. For filling these memories, the selected address source is the output of an address counter which sequentially steps through all 64 addresses.

From either the output of the pipeline register or one of the function memories the data are routed through the positive/negative select circuitry to another pipeline register for timing synchronization. From there the data proceed through the bit precision and bit plane select logic and then out to the D/A converter through the line drivers.

SCANNER III

In order to maintain compatibility with the physical size requirements of the RCA TDI imager to be delivered in the near future, it was determined necessary to modify the configuration of the scanner table at NOSC. Rather than attempt to alter the second-generation scanner currently in use, it was decided to fabricate a completely new scanner testbed. This will allow much more capability and versatility to be designed in. A tentative layout of the third-generation testbed (designated Scanner III) is shown in figure D11.

(The information in this section is taken largely from reference 2.)

CONFIGURATION

There are several major conceptual changes between the designs of the LDTB currently in use and Scanner III. The most obvious of these are the imager placement, the illumination source, and the electronics placement.

The optical axis of the LDTB is only 2-1/2 inches above the table surface. This prohibited the mounting of the test electronics for the TDI imager delivered under a previous contract with RCA. The optical axis on Scanner III is therefore set at 7 inches above the table surface. This height should accommodate the drive electronics for any imager to be tested on Scanner III.

The illumination nonuniformity has been a significant problem in the first two scanner generations. For this reason a contract has been let to Fairchild, Syosset, for an illumination source similar to the one used on the USPS EDM scanner. Because the design includes 24-inch fluorescent tubes, it is expected that uniformity across the 11.5-inch drum surface will be greatly increased.

Also of concern is the aging process of the tubes themselves. The source currently in use is driven by dc voltage with the polarity reversed daily. It is believed that this may cause migration of phosphor chemicals, leading to additional nonuniformity. The Fairchild design utilizes a 19-kHz ac voltage which it is hoped will alleviate any migration.

The current LDTB has the electronics housed in an enclosure above the optical axis and the power supplies mounted beneath the table between the side rails. This layout does not provide convenient access to the power supplies and limits the travel of the imager along the optical axis (for varying resolutions). Scanner III will have the power supplies and all

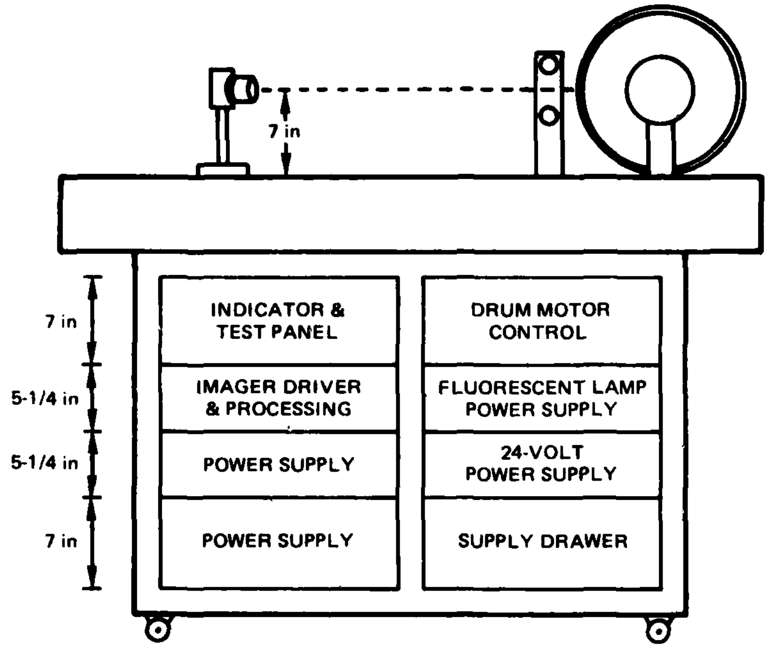


Figure D11. Scanner III.

electronics mounted in a rollabout cart with standard 19-inch racks. This will provide better access to power supplies and more reasonable packaging for both digital and analog circuitry.

With the requirement of 8-bit image acquisition and processing or of a possible increase to 300-pel-per-inch resolution, it will no longer be possible to store a complete 8 1/2-by 11-inch image in the FSM. It is therefore desirable to be able to easily scan portions of a document and to logically "tile" them together to be stored as a contiguous image on tape. To provide this capability, the digital control electronics have been redesigned to allow various image parameters to be set up via the general purpose interface bus (GPIB).

The Scanner III configuration, specifically the use of a new imager electronics circuitry rack, should allow interchangeability of imagers by the simple replacement of an analog and digital card set. Through the use of the TRW monolithic A/D converter(s) within the card set, an improvement in signal-to-noise ratio should be obtainable by accomplishing all analog processing and A/D conversion within one rack. The imagers currently being planned for use in this organization are the Fairchild CCD143 and the RCA TDI imagers.

FAIRCHILD CCD143 IMAGER

The latest-generation linear CCD imager is the Fairchild CCD143, a 2048-element device specified to have blue light sensitivity greater than that of previous devices. The device is specified to operate at up to about 20 megapels per second.

A block diagram of the control and driver electronics is shown in figure D12. This figure is divided into three sections, each representing a different circuit board. Beginning in

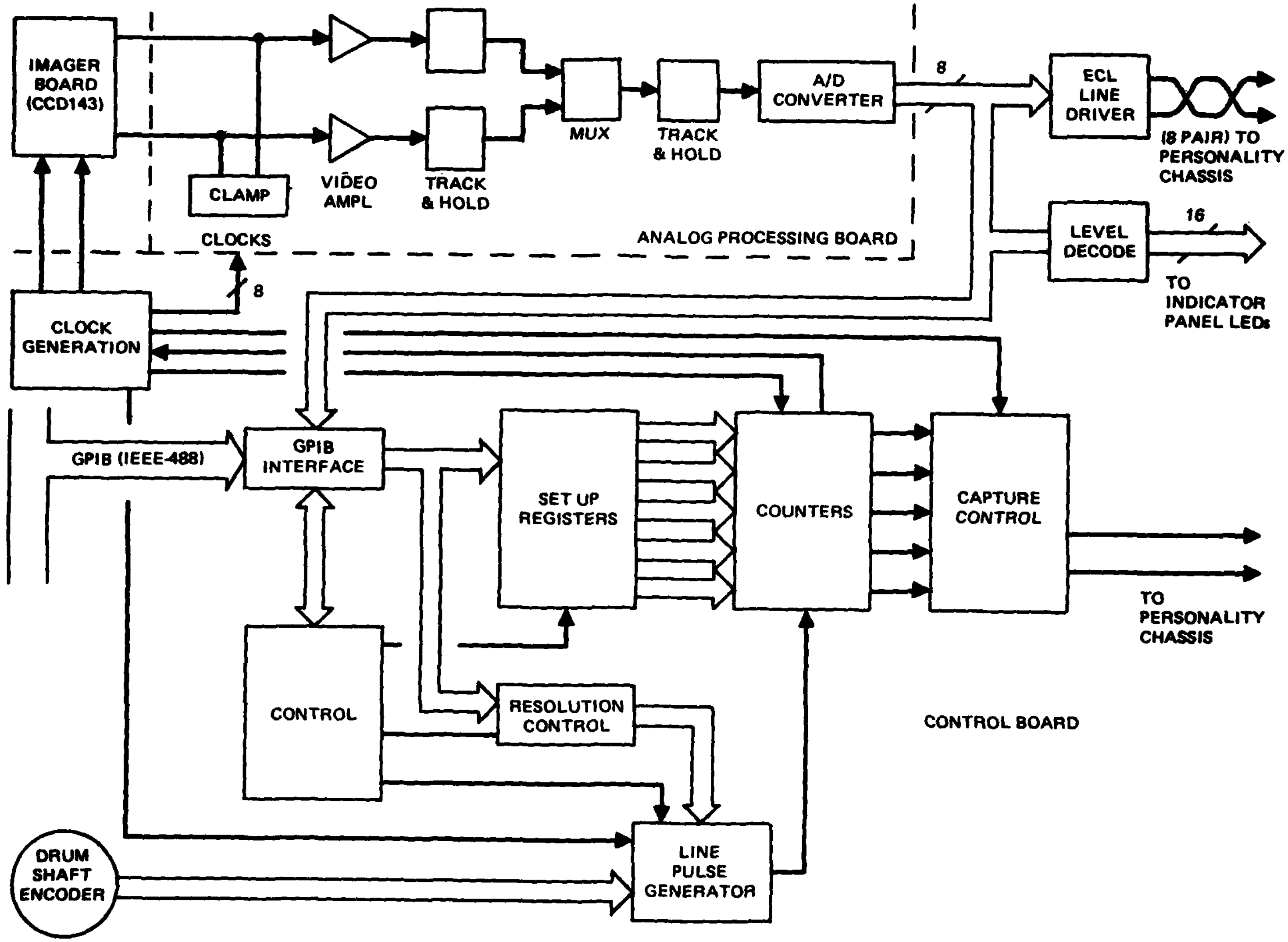


Figure D12. CCD143 control block diagram.

the upper left is the CCD143 driver board onto which the imager is mounted. This assembly in turn is mounted directly behind the imaging lens on the scanner table. This board contains the dc bias voltages and the two required clock signals. The two analog outputs from the imager are fed into buffer amplifiers for transmission to the analog processing board in the card cage.

On the analog processing board, the two channels of video are processed in two video amplifiers, each with a dc clamp circuit. The analog signal at that point consists of essentially return-to-zero waveforms. The two track-and-hold amplifiers are used to sample the incoming waveforms at an optimum rate to provide a continuous analog waveform. The two analog signals are multiplexed to form a single 21-megapel-per-second signal. A third track-and-hold is used to clean up the multiplexed analog signal in preparation for the 8-bit A/D converter. After the signal is digitized, the 8-bit data are routed to the control board for level decoding and for transmission to the personality chassis.

On the control board is a complete general purpose interface bus (GPIB) interface which serves two important functions. First, the GPIB is used to automatically control most of the scanner functions, including vertical resolution select, capture command, number of lines delayed before capture, number of lines to be captured, number of pels delayed on each line, number of pels captured per line, and imager integration time mode select.

This information is stored in the appropriate setup registers. The other primary function of the GPIB interface is to sample the outputs from the A/D converter for linearity testing. For linearity testing, a known analog waveform is input to the A/D converter and the outputs are sampled and transmitted directly to the 4051 for analysis.

Signals from the drum shaft encoder are used on the control board to start the capture sequence and to generate line pulses at the required vertical resolution. The data stored in the setup registers are used to preset a series of counters which in turn are used to control the capture cycle.

TRW 8-BIT A/D CONVERTER

DESCRIPTION

As a part of the continuing effort to improve the quality of imagery acquired by using the ICAS, a TRW 8-bit A/D converter was recently incorporated into the ICAS. It was believed, and, in fact, shown, that by using only the most significant 6 of the 8 bits the TRW device can produce much better linearity than the Phoenix Data converters previously in use. This feature provides both better image quality and better compressibility. Also, with the addition of an 8-bit personality card in the personality chassis, the ICAS will have the capability to acquire, process, display, and print 8-bit images.

The TRW device (TDC1007J) is a monolithic, 8-bit parallel (flash) A/D converter packaged in a single 64-pin dual in-line package. The device is guaranteed to operate at a 20-megasample-per-second rate, but is said to operate typically at up to 30 megasamples per second. It is very likely, then, that four of these converters operating in parallel would handle data from a four-channel imager at the full 84-MHz rate (20 pages per second).

Refer to appendix B of this report for a description of the TDC1007J, its drive circuitry, and the initial device test results.

PERSONALITY CHASSIS

The Personality Chassis (PC) as described in reference 1, appendix A, has undergone several changes and upgrades. The basic operation remains the same, which is to input from one to four pel streams (or channels) of data and demultiplex them in the appropriate order to present a series of 48-bit words to the MIU each containing some number of contiguous pels. These 48-bit words are then sent to the appropriate memory module and stored at an address such that the entire image scanned ends up in a noninterlaced, raster-scanned format.

One new requirement has generated a need for a new strategy in the personality card sets. This requirement involves the accommodation of 8-bit pels in addition to 6-bit pels.

One item discussed in reference 1, appendix A, was deleted from the PC. The MSB-only circuit which is intended to threshold data as they are scanned was not implemented for two reasons. First, the data as scanned are not illumination corrected. Second, assuming that a correction could be performed, level 32 may or may not be the optimum threshold point.

The current block diagram of the PC is shown in figure D13. Data are input from a particular scanner into the corresponding personality card or card set where they are formatted into 48-bit words which are enabled onto a common bus in the PC. The bus includes the three control signals which form a part of all the scanner data interfaces. Those signals are clock, line sync/data gate, data available.

The 51 signals on the bus are then input to two line driver cards, from which the signals are transmitted to the MIU for further demultiplexing into 384-bit words for storage into the FSM.

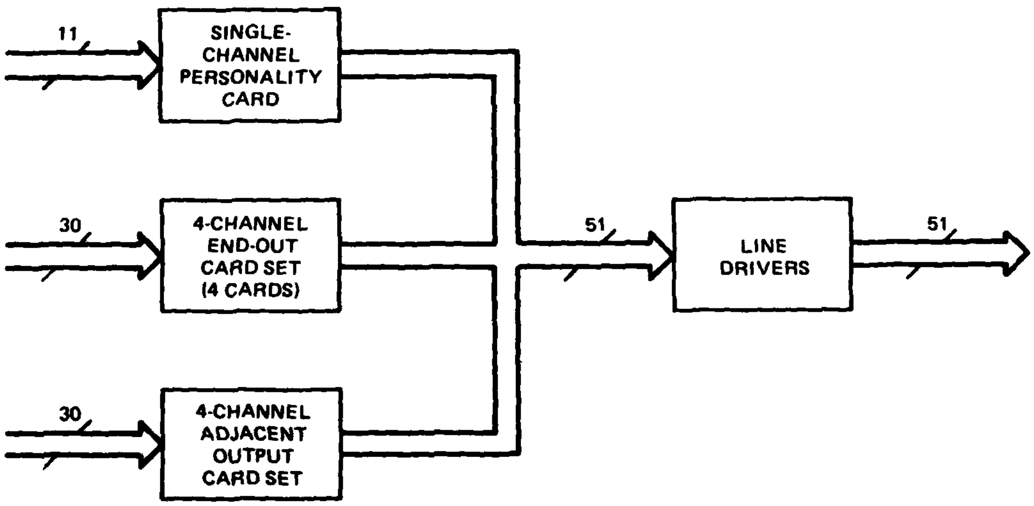


Figure D13. Personality chassis block diagram.

6/8-BIT PERSONALITY CARD

A new single-channel personality card has been designed for the PC which will assemble either six 8-bit pels or eight 6-bit pels into the 48-bit word for transmission to the MIU. A block diagram is shown in figure D14. Eight bits of data and three controls are input as ECL differential signals and immediately translated to TTL levels. The data are then stored in an 8-bit register which can also be used as a test counter for operation verification. From there all 8 bits of data are input to the 8-to-48 demultiplexer while the least significant 6 bits are input to the 6-to-48 demultiplexer. An internal switch then enables one of the two demultiplexer outputs and the PC data bus along with the three control signals.

FOUR-CHANNEL END-OUT CARD SET

The first four-channel personality card set fabricated was intended for application with a new imager developed by RCA–the TDI imager. One of the two possible configurations of the TDI device is a dual 2:1 multiplexer which outputs four pels at a time, two from each end of the image line.

Since that card set was designed, NOSC has been tasked to characterize the Fairchild EDM scanner. The scanner contains two optically abutted CCD131 arrays whose output configuration is identical to the TDI configuration except for the total number of pels per line.

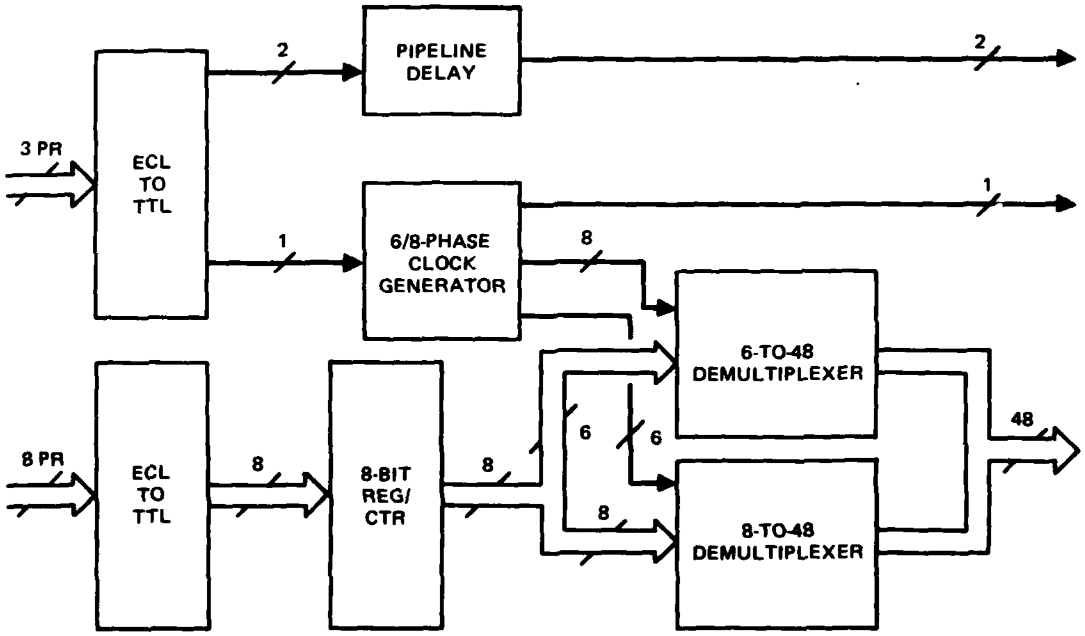


Figure D14. 6/8-bit single-channel personality card block diagram.

The test model of the TDI contains 748 pels per line while the Fairchild scanner contains 2048. In order to use the four-channel card set with the Fairchild scanner, the outputs of the cards had to be rerouted.

In order to store a line of image data, memory must be filled simultaneously from both ends of an image line. This scheme is shown in figure D15. For storage of image data in a DMA mode, the memory is configured into 384-bit words. Thus, to store 2048 pels per line, a total of 32 each 384-bit words is required. For this operation two addresses are generated for words N+0 and N+31. The first address is sent to memory modules 0,1,2, and 3 while the second is sent to modules 4,5,6, and 7. The PC then sends 48-bit words to be stored in the MIU. The first word sent contains the first eight 6-bit pels and goes to module 0. The next word contains the last eight pels on the line and goes to module 7. Once eight words are sent to the MIU, they are stored, half of the 384-bit word at address N+0 and half at address N+31. The address buses are reversed, still with the same two addresses, and eight more 48-bit words are sent, finishing out the first and last 384-bit words. Then the low address is incremented and the high address is decremented, after which the process starts over. This goes on until the last pels are shifted out of each imager, to end up as adjacent pels at the center of the line of image in memory.

The four-channel card set consists of four cards, two of which operate on the first half-line data and two on the second. Figure D16 is a functional diagram of the first card of each pair. This demultiplex module inputs two 6-bit channels of data and assembles groups of four contiguous pels for transfer to the next card in each pair. For example, the card for

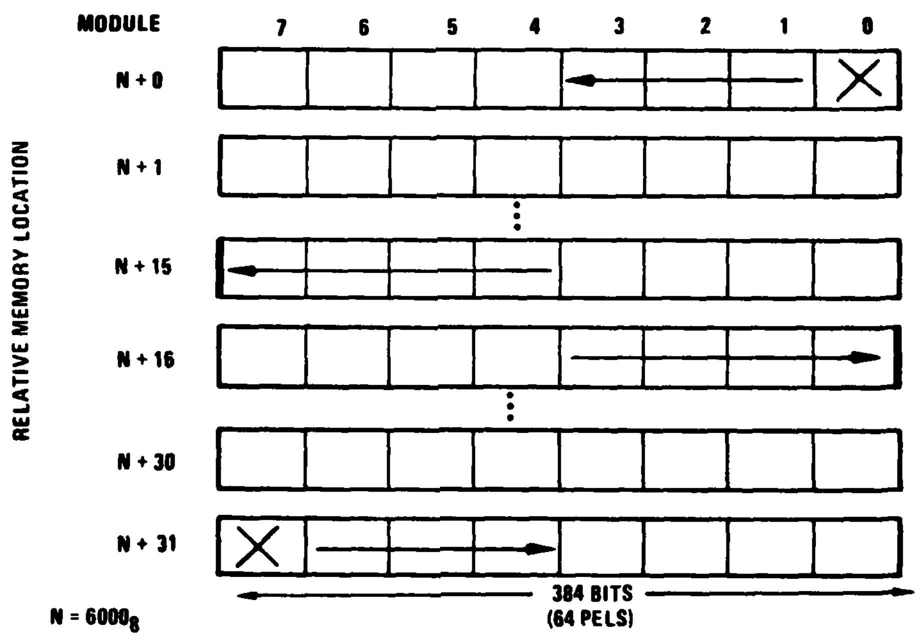


Figure D15. Four-channel pel storage strategy.

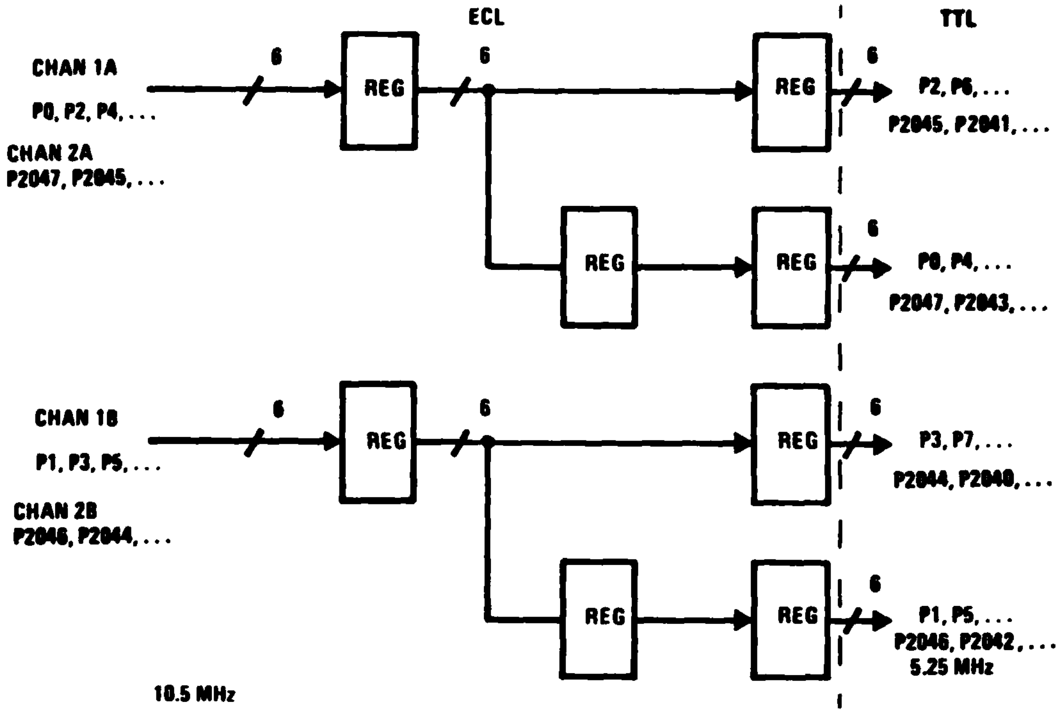


Figure D16. Four-channel end-out card 1 functional diagram.

the first half-line gets pels P0 and P1 followed by P2 and P3, etc. The corresponding card for the second half-line first gets P2047 and P2046 followed by P2045 and P2044, etc. The output of the first card then has P2, P0, P3, and P1, which are transferred in parallel to the next card.

Figure D17 is a functional diagram of the second card in each pair. The pel numbers for the second half-line are omitted for clarity. The groups of four pels input to this card are stored in descending order in each group of four registers. After every two groups of four pels are stored in the registers, the appropriate registers are enabled onto the outputs to provide 48-bit words, each with eight contiguous pels in the proper order. It was the physical wiring of the register outputs to the output pins of each card that needed changing to accommodate the Fairchild EDM scanner. Recalling that a similar card operates on the second half-line data in exactly the same way, the outputs of each card are then sent alternately to the MIU for storage. The first word contains pels P0 through P7, the second word P2047 through P2040, and the third word P8 through P15, etc. This operation, coupled with the addressing technique described, is required to store a complete image in memory in a raster scan format.

No immediate plans have been made to implement an 8-bit-pel version of this card set.

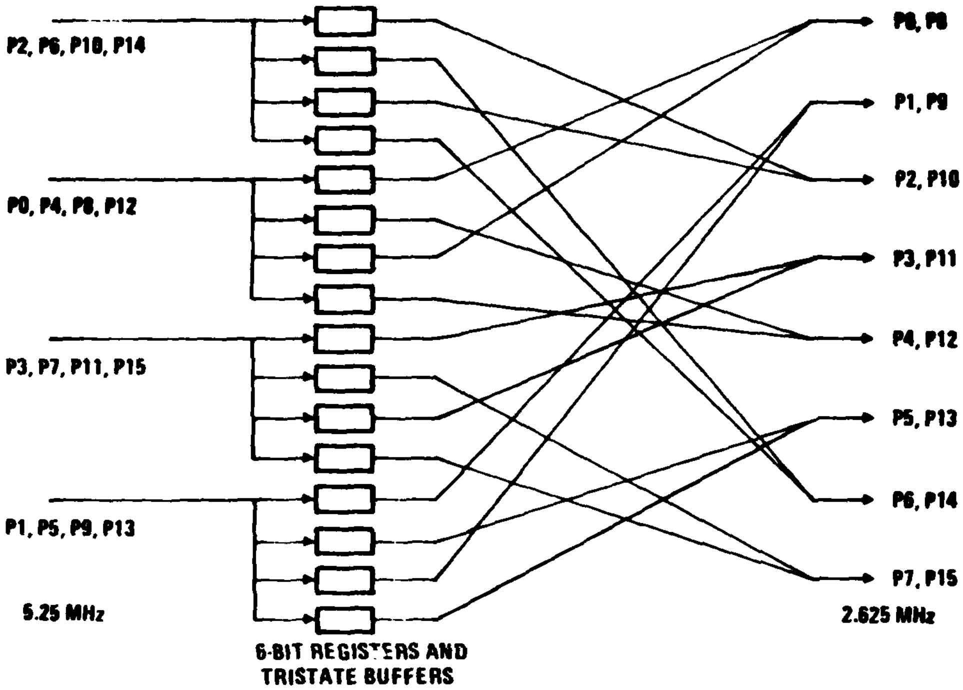


Figure D17. Four-channel end-out card 2 functional diagram.

FOUR-CHANNEL ADJACENT OUTPUT CARD SET

The primary intended output configuration of the TDI imager is a four-channel output in which four adjacent pels are available at a time, P0, P1, P2, P3 followed by P4, P5, P6, P7. This represents a much simpler task for a personality card and also requires only a single address for the FSM. The design of this card set is in progress and the block diagram is shown in figure D18. For 6-bit data all that is required is a 24-to-48 line demultiplexer. However, this requires at least two cards because of I/O pin limitations. Plans are being considered for implementing a 6-bit/8-bit card set to operate with either 6-bit or 8-bit data.

ANALOGIC DIGITAL TO ANALOG CONVERTER

As of the beginning of FY80, the sole remaining item of government furnished equipment (GFE) in ICAS was the Motorola D/A converter used to produce display video for the Conrac RQB monitor. That converter was recently replaced with an Analogic MP8308 ultra-fast converter.

The Motorola converter was a 100-MHz device which used ±5 V and ±15 V. The Analogic converter is also a 100-MHz device, but uses only ±5 V. The Motorola device was

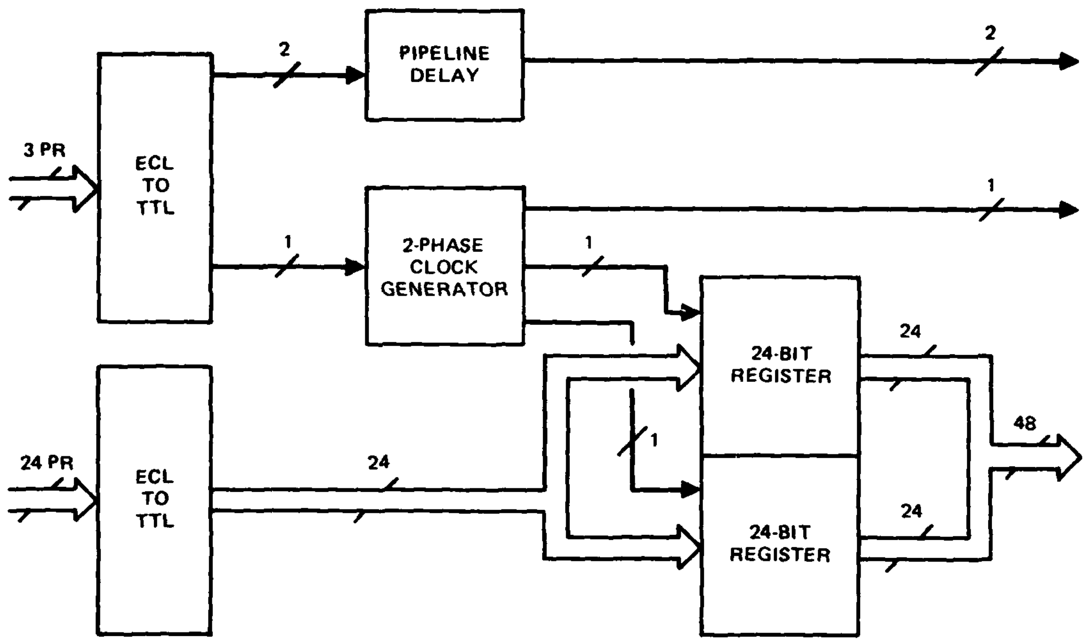


Figure D18. Four-channel adjacent output block diagram.

strictly a D/A converter. A separate amplifier was required to provide sync and blanking signals. The Analogic device has sync and blanking as inputs and provides composite video as an output.

Although the Motorola unit accepted 10-bit input, only the upper 6 were used. The 8-bit input of the 8308 is sufficient even if it is decided to accommodate the display of 8-bit images. In addition, the bandwidth will be sufficient should it be decided to convert to a 1024-by-1024 display.

FUTURE PLANS

Since the algorithm for illumination correction was originally implemented in software, the intent has been to develop a hardware implementation. At one time, a design had been generated; however, the design was not space-efficient and the speed requirements for memory devices exceeded the capability of available technology.

HARDWARE ILLUMINATION CORRECTOR (HIC)

Technology has caught up with the speed requirements of the HIC. It has therefore been decided to fabricate a single-channel (21-MHz) HIC to be incorporated into the ICAS.

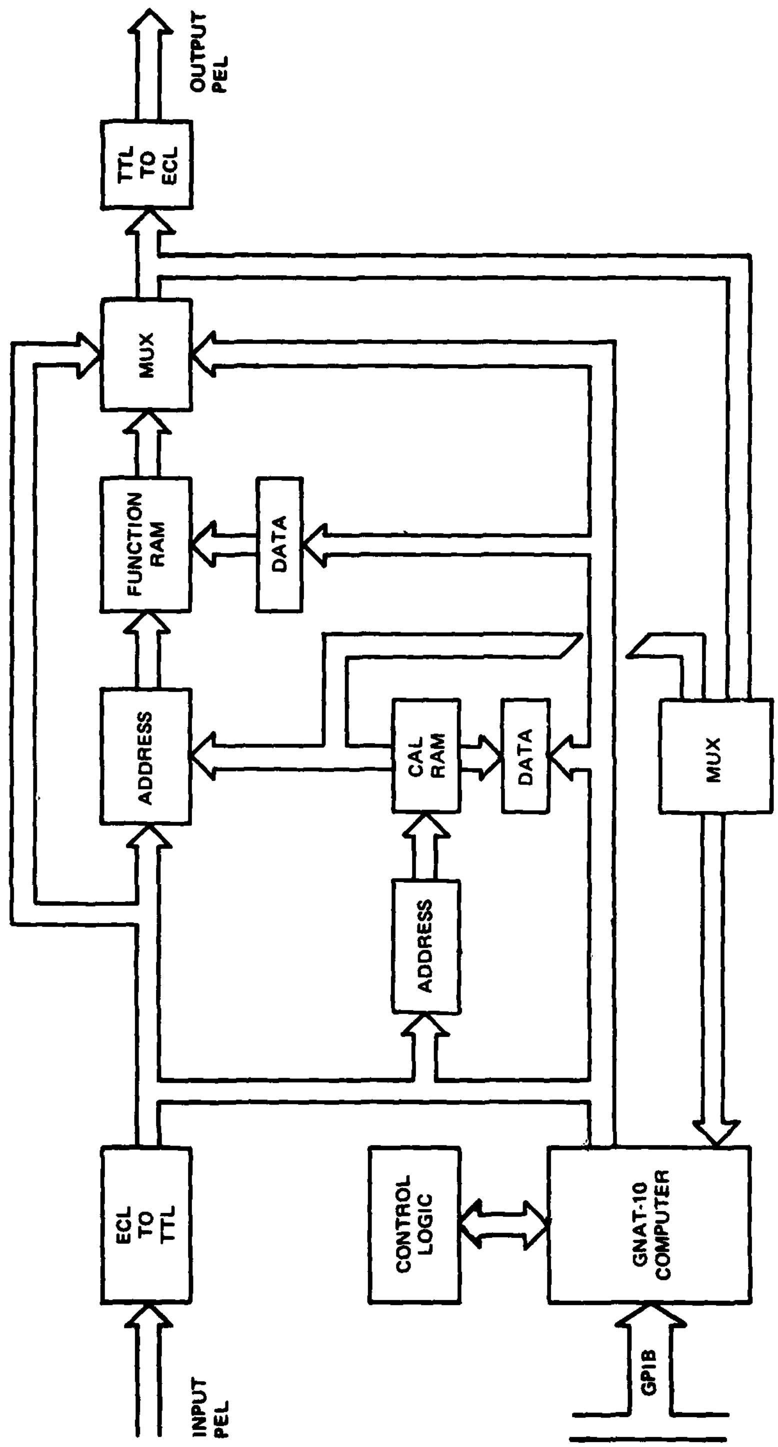


Figure D19. Hardware illumination corrector block diagram.

A contract has been awarded to Data/Ware Development, Inc (San Diego), for the design and fabrication of this unit. The preliminary design has been completed and some of the components have been acquired by DWD.

The DWD approach to the hardware design is basically the same as the original NOSC approach but takes advantage of newer technology to provide greater speed and more versatility. A block diagram of the HIC is shown in figure D19. (For details on the correction algorithm, see reference 3, appendix A.)

The HIC is controlled by a Gnat-10 stand-alone minicomputer. This computer will be added to the GPIB as an extension of the existing multiprocessing system. Calibration and function data will be passed from either the 4051 or the MCU to the Gnat, which in turn will pass the data to either the calibration (CAL) RAM or the function RAM. The HIC is organized in a manner such that the correction function may be bypassed or such that pel or RAM values may be read by the Gnat. Also, the Gnat can generate test data and input results of the function to check the hardware operation.

An additional feature of the HIC in its current design is the use of RAM rather than ROM for the function memory as in the original design. This means that any function may be loaded into the RAM—eg, illumination correction—with that result thresholded at any desired level.

HARDWARE EDGE ENHANCER (HEE)

The contract to Data/Ware Development also includes a requirement for the design and fabrication of a hardware edge enhancer. The design for this unit is still in the preliminary stage but follows the algorithm described in reference 4. The Gnat computer used to control the HIC will also be used to control the HEE. Provision will be made for a variable gain constant and for stand-alone testing as in the HIC.

STAND-ALONE SYSTEM

As of this writing, USPS has placed an order for a Tektronix 4054 graphic system, a 4907 file manager, and a 4641 matrix printer. These additions to the equipment being used at NOSC are expected to greatly increase the throughput capability of the ICAS as described below.

The 4054 will replace the 4051 currently in use by the ICAS. The 4054 has several features that make this desirable. The 4054 is directly upward compatible (in software) with the 4051, yet has between a fourfold and a tenfold increase in instruction execution speed. This does not necessarily indicate an equivalent increase in overall throughput but does indicate that for certain mass data operations such an increase may be possible. The 4054 has a faster, more versatile graphics capability than the 4051, which should allow an increase in throughput of results display, as well as an improvement in quality.

The ICAS, partially through its own versatility, has frequently become a bottleneck for the completion of tasks. In addition to image acquisition, processing, and output, ICAS is used for software development, data base management, and hardware test and control, among other things. The 4051 being replaced, used in conjunction with the additional 4907 and the 4641 printer, will be used as a stand-alone system, which will eliminate a significant portion of the competition for ICAS usage.

The most significant portion of ICAS usage has been devoted to image processing and software development. The task completion cycle has characteristically been serial, or leap-frog, in nature. A task would be assigned, software developed, and processing executed. With the formation of the stand-alone system, this sequence can be turned into a largely parallel operation. While execution of one task is carried out on the ICAS, software can be developed on the stand-alone system for the next task. The only time required on the ICAS for program development should be a minimal time for debugging of MCU software.

Other functions that can be allocated to the stand-alone system include, but are not limited to, microcode (PROM) maintenance, some hardware test control, data base maintenance and inventory maintenance. Figure D20 is a block diagram of the projected stand-alone system.

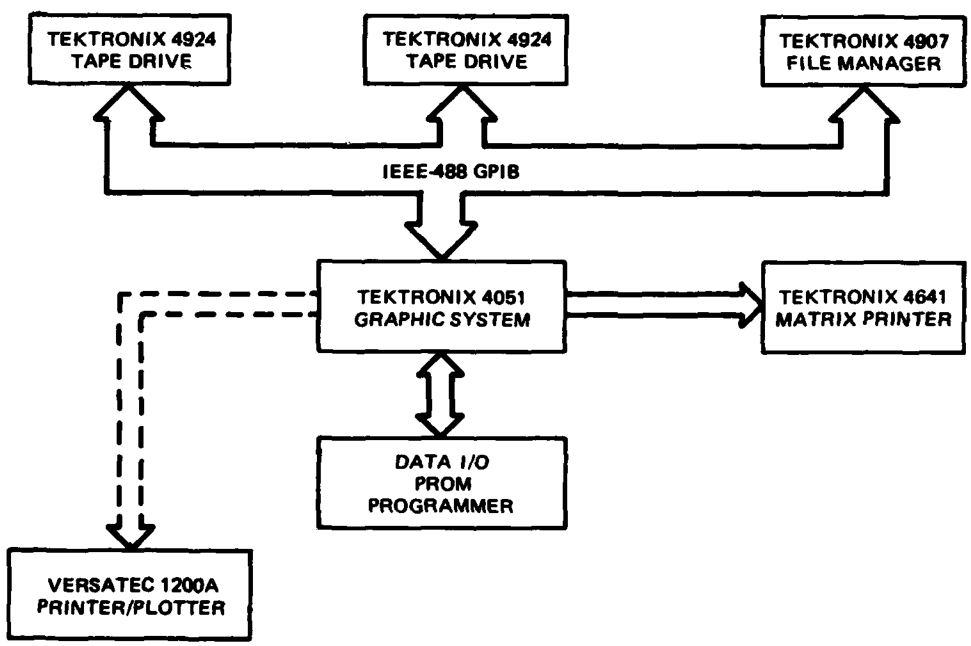


Figure D20. Stand-alone system projected block diagram.

SUMMARY

It should be obvious from the preceding information that the ICAS has grown considerably in capability and versatility since the FY77 report. There has been an increased tendency toward modularity in both hardware and software in order to ease transition between tasks. This includes modification of portions of the ICAS for specific tasks as well as for altered direction of primary interest in the area of imaging.

Table D3 gives a brief comparison of the equipment incorporated into ICAS in FY77 and FY80.

Function	FY77 Configuration	FY80 Configuration
System control	Tektronix 4051	Tektronix 4051 (4054*)
Program storage	Magnetic tape	Tektronix 4907 File Manager
Image acquisition	2nd generation scanning table	3rd generation scanning
Imager	CCD121	CCD121H, CCD143,*
A/D converter	4 each Phoenix Data 1106	TDI*, TRW TDC1007J
Image display		
Monitor, monochrome	Conrac RQB17/C	Conrac RQB17/C
Monitor, color	none	SRL model 374
Control	Firmware	Hardware
D/A converter	Motorola 100 MHz	Analogic 100 MHz
Color image processor	none	Comtal Vision One
Bilevel printing	none	Versatec 1200 A
Color printing	none	Dicomed D47

*Planned for near future

Table D3. ICAS equipment summary.

APPENDIX E:

TDI CCD IMAGER STATUS

by

Lee A Wise

Code 7323

September 1980

CONTENTS

ILLUSTRATIONS

INTRODUCTION

As a significant step toward meeting the EMS goal of scanning 8 1/2-by-11 inch pages at a rate of 20 pages per second, two contracts have been awarded to RCA Laboratories, Princeton, New Jersey, for development of a CCD page reader satisfying this requirement. The first of these contracts was awarded by NOSC (contract N00173-76-C-0980) on 15 March 76, and ran until 15 May 77. The second contract, a continuation of the same development effort, was awarded by USPS (contract 104230-79-Z-1613) on 18 July 79 and is in progress.

This development effort includes the design, fabrication, and testing of a small-scale CCD device operating in the time-delay and integration (TDI) mode. The development model contains 96 rows of 748 photosites which can then be scaled up to 2200 photosites in order to scan the 11-inch dimension of each page.

This report includes a summary of the first contractual effort and the current status on the second contract, as well as NOSC plans for testing the devices to be delivered at the end of the second contract phase 1 effort.

BACKGROUND

The initial phase of the first contract consisted of design tradeoffs for both the imager configuration and the type of gate structure used in the active imaging area. The result of the tradeoff study is a test device configured as shown in figure E1. The active imaging area consists of 96 lines by 748 pels per line using a two-level polysilicon buried-channel CCD structure. The clocking scheme uses a four phase electrode-per-bit TDI clock. For this development chip, two options may be exercised for readout of the image data. At the bottom of figure E1 is a 4:1 multiplexed output register configuration. With this configuration, four adjacent pels are output at one time via four separate output registers. It is expected that these output registers will operate at 21 MHz, but there is a possibility that, due to the relatively large stage length (2.4 mils) of these registers, the charge transfer efficiency will be too low for satisfactory operation. A second option is shown at the top of figure E1. To use this alternate output option, the device is physically turned upside down and the TDI section is clocked in the reverse direction. This output consists of a double 2:1 output multiplexer and four output registers, each reading data from the edge of the image area toward the center. The advantage of this gate structure is that the stage length of these output registers is 1.2 mils, half that of the 4:1 multiplexed output registers. For a given clock frequency, the shorter stage length should provide a higher charge transfer efficiency.

In the imaging area the effective pel-to-pel spacing is 0.6 by 0.6 mil. The horizontal resolution is defined by 0.4-mil CCD channels and 0.2-mil channel stops. In the vertical dimension, the TDI gates are designed with 0.35-mil gates and 0.1-mil spaces for a gate-to-gate spacing of 0.45 mil. To calculate the effective resolution refer to figure E2. This figure shows the timing relationship between four phase electrode-per-bit clocks and the charge packets as they are clocked through the imager. There are three charge packets being integrated for every four gates. Considering the charge packet labeled 1 in figure E2, it is seen that it is integrating charge under a single gate. 2 is turned on, enabling the charge packet to move to the potential well under gate 2. During this time period the effective window is two gates wide under which charge is accumulated. This cycle is then repeated as each charge packet is clocked vertically through the imager. The effective resolution center-to-center pel spacing can be shown to be four-thirds L, where L is the center-to-center gate spacing, or 0.6 mil.

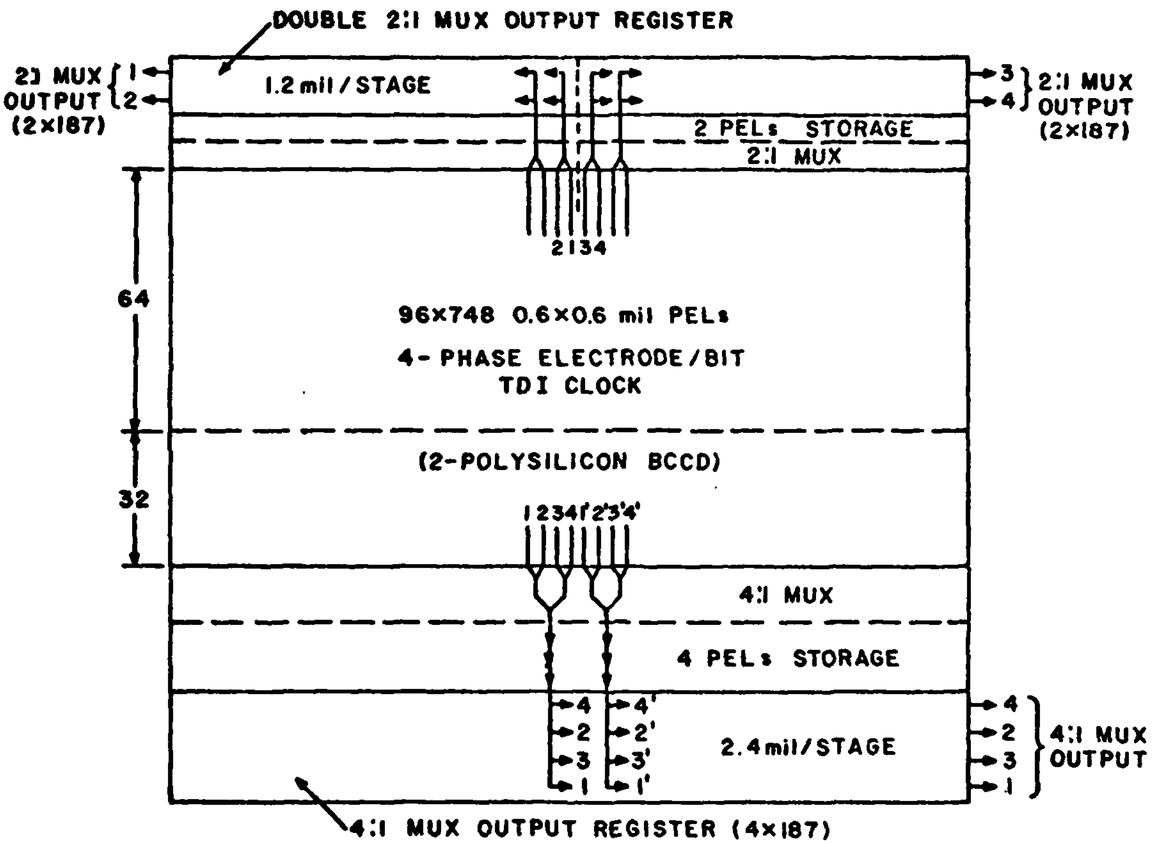


Figure E1. Block diagram of TDI image sensor.

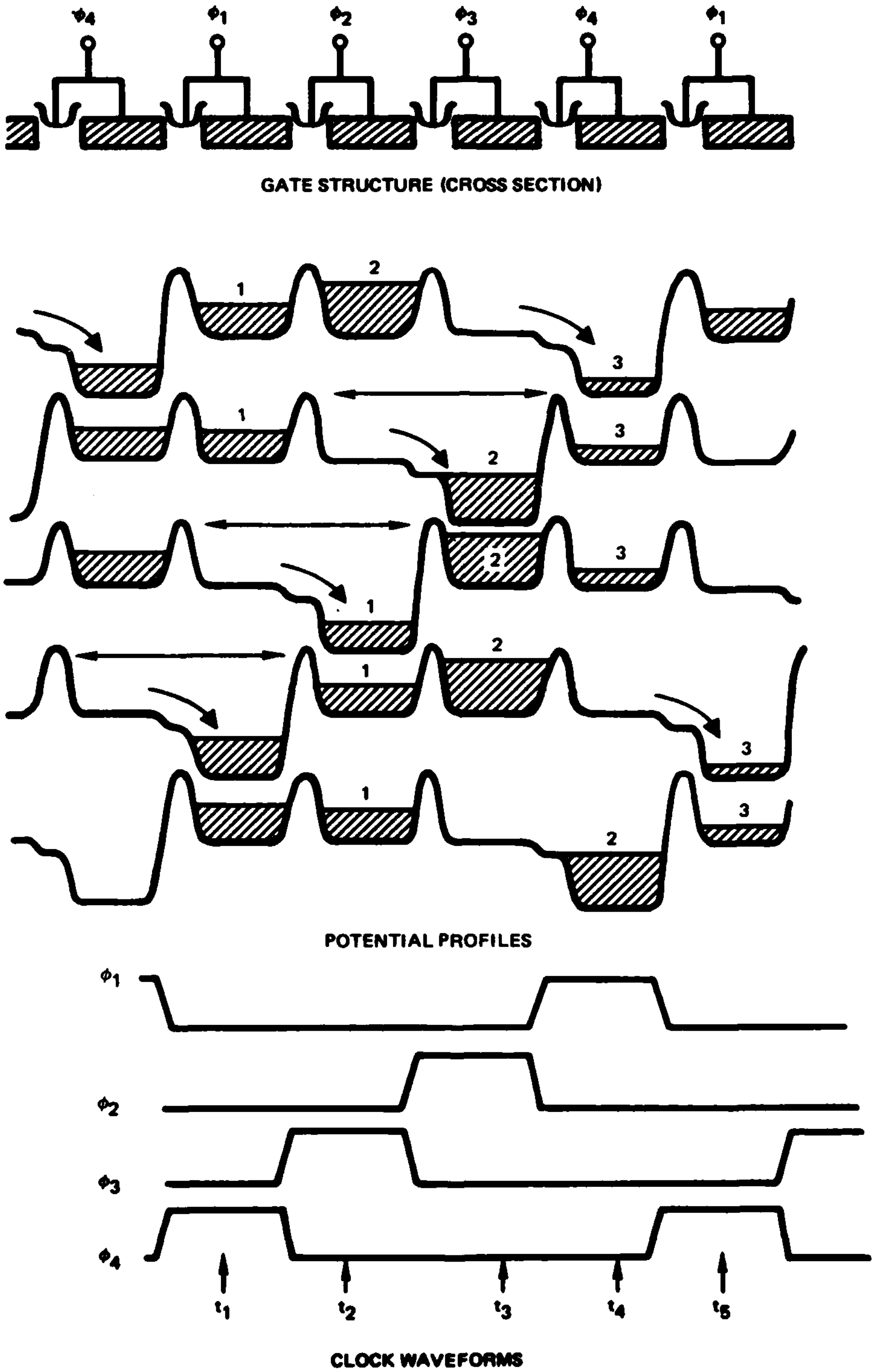


Figure E2. TDI gate structure and clocking waveforms.

The mask set for the chips was made by a laser-controlled photocomposition machine. Since the TDI device is so large, 528 by 232 mils, three different reticles were required for the step-and-repeat photocomposition process. This introduced a small alignment problem which was held to less than 0.02 mil. With this mask set three processing runs were made, the third of which produced 11 devices with some optical output.

The devices were bonded in 56-pin flatpack packages. These presented a considerable problem when wire-bonding. The imager chip surface was not on the same level as the flatback bonding pads, which required refocussing of the microscope when making each bond. A rather complex waveform generator was designed and fabricated for driving the TDI imagers. The electronics had to produce five sets of waveforms:

TDI electrode-per-bit clocks

4:1 multiplexer clocks

Temporary storage register clocks

Output register transfer clocks

Output register clocks

Each of the clock signals generated had to have separate dc bias and amplitude controls to operate the imager properly. The electronics was implemented with hard-wired logic and was designed only to operate the TDI imager in the 4:1 multiplexed output mode. Also, the testing of the devices did not actually involve tracking a moving image. Instead, a stationary image was used and a strobe light essentially "flashed" the image onto the imager. The resulting image was then clocked down the imager and shifted out of the 4:1 multiplexed output registers. RCA successfully demonstrated that the imager did produce an image in this manner.

STATUS OF CURRENT RCA EFFORT

The major milestones of the first phase of the second contract with RCA include:

Development of improved test equipment for 748-by-96-element TDI arrays

Transfer loss measurements of 4:1 multiplexed output register for clock frequencies of 1 to 21 MHz.

New mask generation for 748-by-96-pel arrays

Delivery of 10 devices

The assembly of new TDI driver electronics is nearly complete. This very flexible design uses high-speed Schottky TTL random access memories (RAM) for storage of the 21 different waveforms required for operation of the TDI imager. This technique allows easy modification of the waveforms in order to optimize the TDI operation. To generate the waveforms, load into RAM, and store and retrieve them from a cassette tape, an RCA COSMAC VIP (video interface processor) was used, which is a complete microcomputer on a single board. A CRT monitor is used for display of commands and of the encoded waveform data during generation of the data or upon retrieval from tape.

Once the waveforms are stored in RAM, high-speed clocks are enabled which read the data out of the RAM and generate the special clock waveforms which are then sent to the TDI driver board. The TDI driver board contains clock driver circuits along with adjustable voltages and clamp circuits for each clock signal. The Motorola M0026 MOS clock driver circuit is capable of driving most of the clock signals. However, for the four output register clocks that must run up to 21 MHz the M0026 will not work. Currently, RCA is implementing a clock driver circuit incorporating a National Semiconductor Damn Fast Amplifier (LH0063) which is capable of 21-MHz operation driving a 350-pF load.

In order to test the TDI chips in the tracking mode, NOSC supplied RCA with a large drum test bed (LDTB) containing a 40.96-inch-circumference drum, shaft encoder, and drive motor (figure E3). Also, in order to synchronize the operation of the TDI chip with the motion of the drum, a phase-locked loop (PLL) circuit was designed by RCA which runs at 128 times the line rate. This PLL accurately tracks the variation in the drum speed on the LDTB, which is less than $\pm 0.5\%$.

Some testing was performed on the 4:1 multiplexed output register on one of the TDI chips from the previous contract. At frequencies up to 5 MHz there was negligible transfer loss. At 10 MHz the transfer loss measured to be approximately 5×10^{-5} per transfer. When the frequency was increased to 15 MHz, the transfer loss was measured to be something less than 10^{-4}, but considerable ringing was observed on the clock lines. An attempt was made to rewire the TDI socket using shorter lead lengths, but afterwards the operation of the tester became intermittent. At that point further testing was suspended in favor of processing new TDI chips for testing with the new electronics package.

During the time intervening between the two RCA contracts, a new Manufacturing Electron Beam Exposure System (MEBES) for mask generation was installed at RCA, Somerville, NJ. In order to use this system to generate a new mask set for processing TDI chips, the old artwork tape used previously had to be converted from English units to metric units. During this conversion, many roundoff errors occurred, some of which were fatal to the design. Two areas that required reworking were the TDI section and the 2:1 multiplexed output section. These areas were corrected and the new tapes were sent to Somerville for the mask generation. The MEBES produces an entire mask in one operation, as opposed to generating three reticles and then photocomposing the step-and-repeat master with its inherent alignment problems.

During the processing of the first run of wafers a few problems occurred which affected the active imaging area. However, testing of the 4:1 multiplexed output section could be carried out. At a frequency of 1 MHz the charge transfer inefficiency was estimated at 7×10^{-5} per transfer. The uniformity of the four output registers was found to be better than that of the previous devices. Several problems discovered in the first run have been corrected for the second run, which is still in progress.

New improved lead frames have been purchased for the new runs of TDI chips. They are 64-pin dual in-line packages. With the chips in place, the bonding pads are on the same level as the lead frame, greatly easing the bonding task.

NOSC EVALUATION PLANS

NOSC has in fabrication a new large drum test bed (LDTB), designated Scanner III. It is the third-generation drum scanner designed and fabricated at NOSC for testing imaging devices and systems. During FY80, NOSC built and delivered a similar scanner table to RCA, Princeton, for their use in testing the TDI imagers. Figure E4 is a diagram of Scanner III.

Several major improvements have been incorporated into Scanner III. The optical axis on the table has been raised from 2.5 inches to 7 inches in order to more readily accommodate the TDI imager and its driver board with the high-speed clock driver circuits. A new illumination source has been purchased from Fairchild Weston Systems, Syosset, for use on the LDTB.

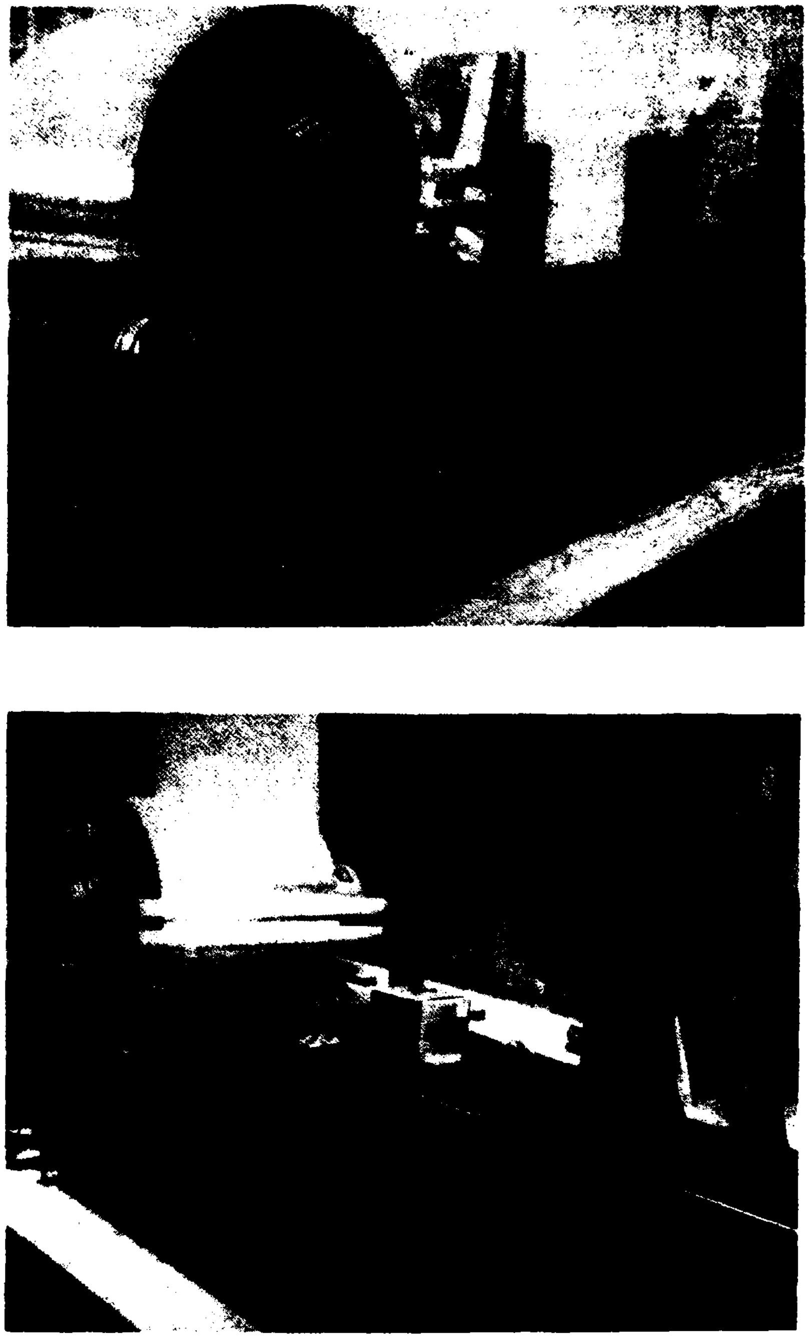


Figure E3. Large drum test bed.

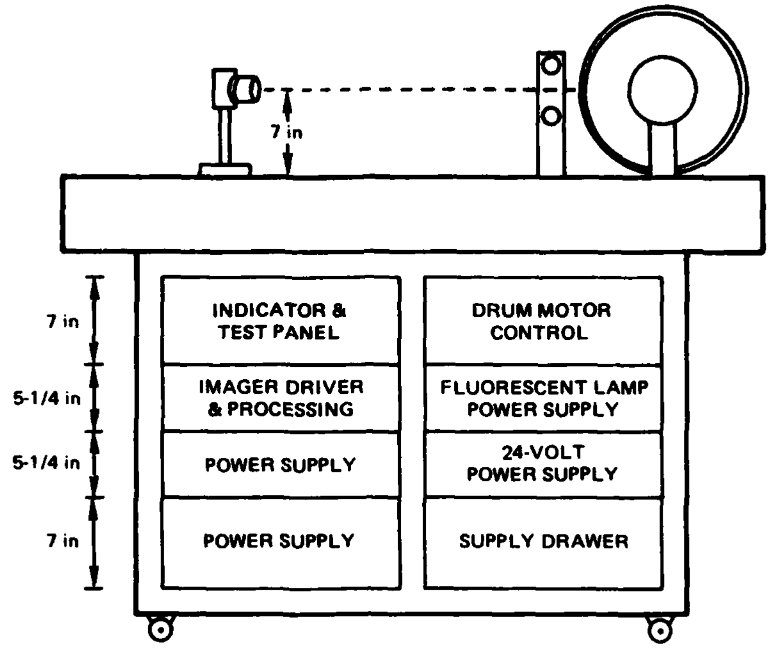


Figure E4. Scanner III.

It utilizes two 24-inch slit-aperture fluorescent tubes. The cylindrical enclosures for the tubes contain light guides and cylindrical Fresnel lenses which focus the light into a relatively small area on the surface of the drum. The lamps are powered by a 19-kHz ac power supply, which will provide flicker-free illumination and prevent any appreciable phosphor component (mercury) migration from one end of the tube to the other.

The scanner electronics, power supplies, and motor controls are housed in a rollabout cart which contains two 19-inch rack-mount sections, each 24.5 inches high. The electronics card cage can hold up to four 9-by-15-inch circuit cards. The design of the electronics will allow different card sets to be used in this card cage for each different imager used on the LDTB. A two-card set has been designed for the CCD143 2048-pel linear array. It is expected that four cards will be required for operating the TDI imager chip.

TDI SUPPORT ELECTRONICS

Figure E5 shows a block diagram of the control and analog processing circuitry planned for testing the TDI imagers. The TDI driver board set will be supplied by RCA as a deliverable. This board set consists of two PC boards one of which contains all the low-speed clock drivers and their respective amplitude and bias controls in addition to the imager itself. The second board contains the four high-speed clock driver circuits and their respective controls.

For generation of the approximately 21 waveforms required to drive the TDI, the RAM circuitry used will be similar to that which RCA developed. However, it will be packaged differently in order to be compatible with the Scanner III electronics card cage. As shown in figure E5, all the RAMs, the phase-locked loop circuit, and the high-speed clock generator will be placed on one 9-by-15-inch wirewrap board, the TDI waveform generator board.

To generate and store the waveform information, the ICAS terminal and floppy disk system will be used in much the same way that RCA utilizes the microprocessor board and cassette recorder. In ICAS, however, the data will be transmitted via the PIGB to the TDI digital control board in Scanner III. This board contains a GPIB interface which will route the RAM data into the proper channel. Also contained on this board are the necessary setup registers and scan control counters used for controlling the image capture sequence. The outputs from the capture control circuits are the data available and the line sync/data gate signals. The shaft encoder interface will reside on the TDI digital control board and be used to control the vertical resolution during scanning.

For processing and digitizing the four channels of analog data, two 9-by-15 inch cards will be needed. Each of these cards will include two video amplifiers with dc clamp circuits capable of 20-MHz operation. The outputs of the video amplifiers will be converted to 6-bit digital data by two TRW A/D converters, each of which is capable of 8-bit conversion at up to 30 MHz. From this point the digital data will be transmitted to the ICAS personality chassis, where it will be formatted into 48-bit words for storage in the frame-store memory.

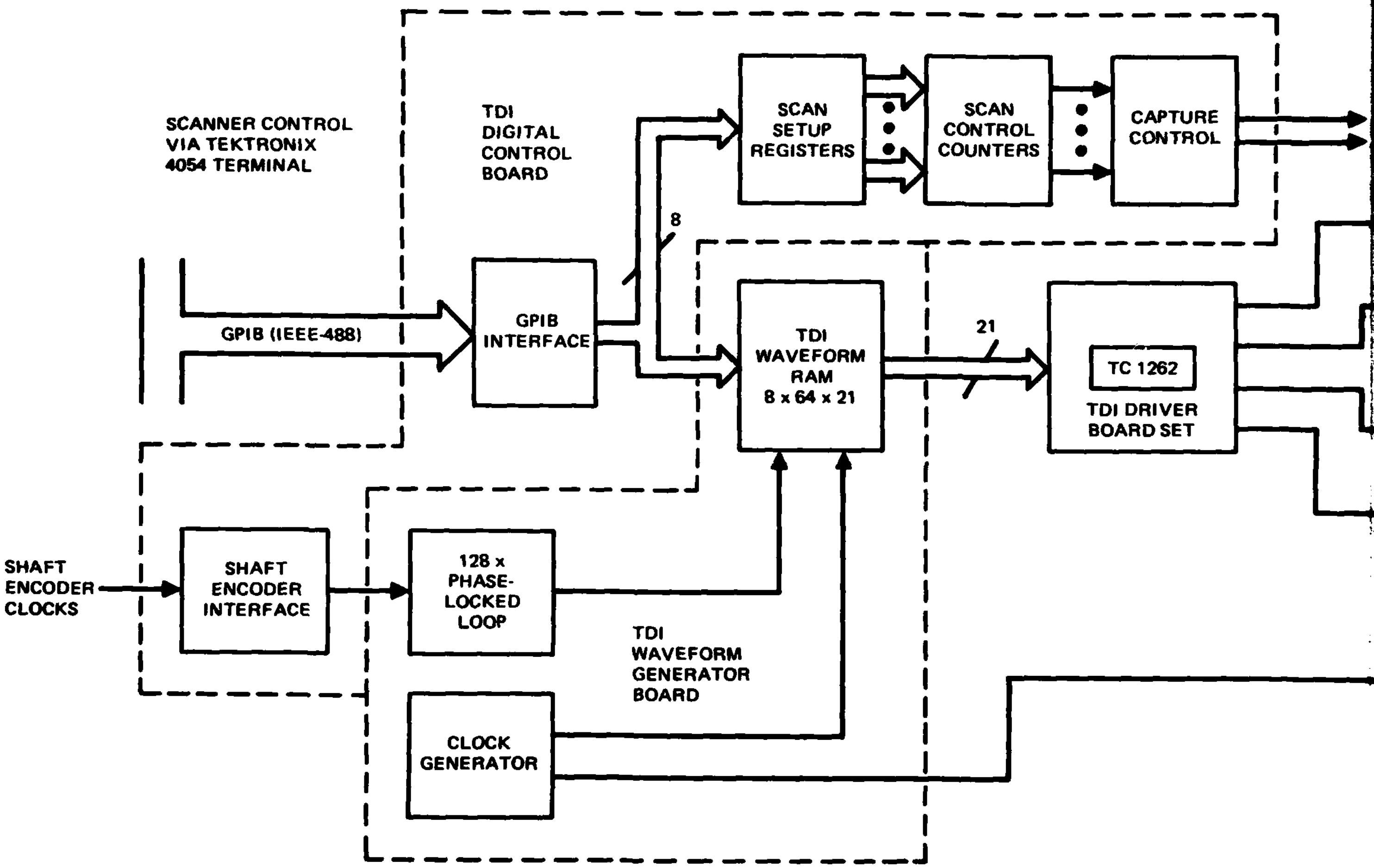
As mentioned previously, there are two options for reading image data out of the TDI imager. The more straightforward approach, from the point of view of data manipulation, is the 4:1 multiplexed output. However, to completely characterize the TDI imager, the 2:1 multiplexed outputs should also be tested. In order to test the two different output options, the chips themselves must be wire bonded for a specific output option. There are not sufficient pins on the lead frames for bonding both types of outputs simultaneously. In addition, a different driver board must be built to accommodate the second option. The same number of waveforms must be required for the 2:1 multiplexed outputs as for the 4:1 multiplexed outputs, so that the same waveform generation RAMs may be utilized, only with a different set of data.

In order to accommodate both types of outputs, two different card sets are required in the personality chassis. A card set for the 2:1 multiplexed output configuration has been tested and used with the Fairchild EDM scanner subsystem. The more straightforward card set for the 4:1 multiplexed output configuration is currently in design.

PLANNED TDI TESTS

RESOLUTION AND TRACKING ABILITY

One of the most important questions concerning the TDI operation is: how well can the TDI imager "track" an image as it moves across its surface? Planned tests involve scanning a test image which contains very well defined horizontal lines approximately 0.005 inch in width. For one test, a portion of the image will be "flashed" onto the imager with a strobe light and then shifted out of the imager and stored in memory. Following that test, the same image will be scanned in the tracking mode and stored in memory. Then the two images may be compared for smearing or a lack of definition of the sharp edges in the image.


SCANNER CONTROL
VIA TEKTRONIX
4054 TERMINAL
TDI
DIGITAL
CONTROL
BOARD
SCAN
SETUP
REGISTERS
SCAN
CONTROL
COUNTERS
CAPTURE
CONTROL
8
GPIB (IEEE-488)
GPIB
INTERFACE
TDI
WAVEFORM
RAM
8 x 64 x 21
21
TC 1262
TDI DRIVER
BOARD SET
SHAFT
ENCODER
CLOCKS
SHAFT
ENCODER
INTERFACE
128 x
PHASE-
LOCKED
LOOP
TDI
WAVEFORM
GENERATOR
BOARD
CLOCK
GENERATOR

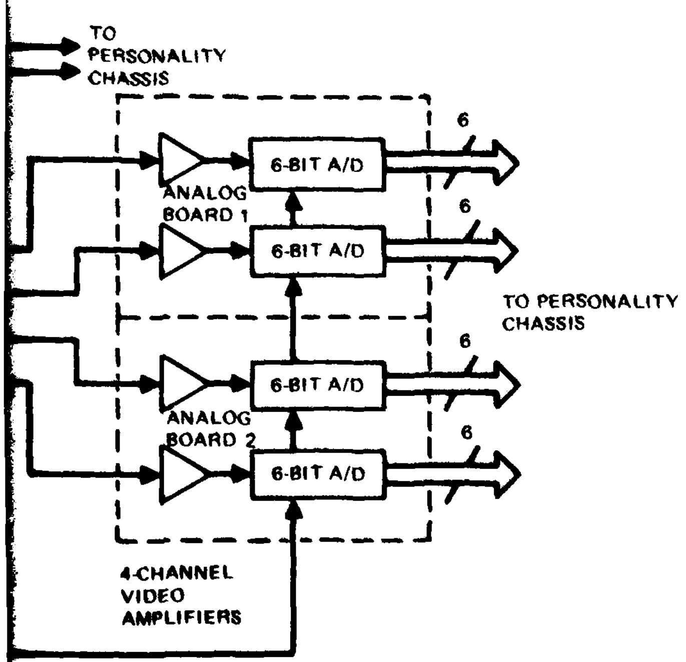


Figure E5. TDI imager and support electronics.

SPECTRAL RESPONSE

The spectral response of the TDI imager may be checked with the use of the Gamma Scientific scanning spectroradiometer equipment. A calibrated light source is used with a monochromator to scan the visible spectrum. The output of the monochromator is then shown onto the imager. The imager output is recorded for all wavelengths, thus producing a plot of the total spectral response. These data can also be used to calculate the device responsivity, which is the output signal voltage per unit exposure for a specified spectral type of radiation.

PHOTORESPONSE UNIFORMITY

The uniformity of response of the entire 748-by-96-pel array may be evaluated by means of a strobe light. After one strobe flash, the resulting image can be read out and stored in memory for analysis. This will show bad cells or columns of cells in the array and their exact locations as well as the uniformity of response across the imager. These outputs will also be examined for any effects of the charge transfer inefficiency in the output shift registers.

PERFORMANCE VERSUS SPEED OF OPERATION

It is planned to test the TDI devices at a minimum of three speeds equivalent to approximately 5, 10, and 20 pages per second. Performance factors such as uniformity of response, dynamic range, resolution, and output image quality will be examined for the different speeds of operation.

DYNAMIC RANGE

The dynamic range will be computed for each device at all frequencies tested. The dynamic range will be computed by dividing the saturation exposure by the peak-to-peak noise equivalent exposure, which is defined as the exposure level which gives an output signal equal to the peak-to-peak noise level output with zero exposure.

FOUR-CHANNEL UNIFORMITY

For both the 4:1 and 2:1 multiplexed outputs, the uniformity of the four output shift registers will be measured. This will be done at NOSC with uniform illumination of the imager. These results will be compared to RCA's test results using an electrical input to each of the registers.

TIME AND TEMPERATURE STABILITY

Stability of not only the TDI device itself but of all the supporting electronics is of great importance in this application. The stability of all the circuits around and including the

TDI imager will be monitored closely. The video amplifiers used in this application have been chosen with stability as an important criterion. The need for this was clearly demonstrated after testing the previous designs of amplifiers in the ICAS.

CONCLUSIONS

The highlights of the first RCA TDI imager contract and the current status of the present contract with RCA have been presented here. It is expected that RCA will deliver a series of TDI imagers that will demonstrate the ability to perform TDI scanning at an effective 20-page-per-second rate.

Plans for the testing of the TDI imagers at NOSC have been detailed here. The implementation of the control circuitry is currently in progress and it should be ready for testing when the TDI devices are delivered.

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